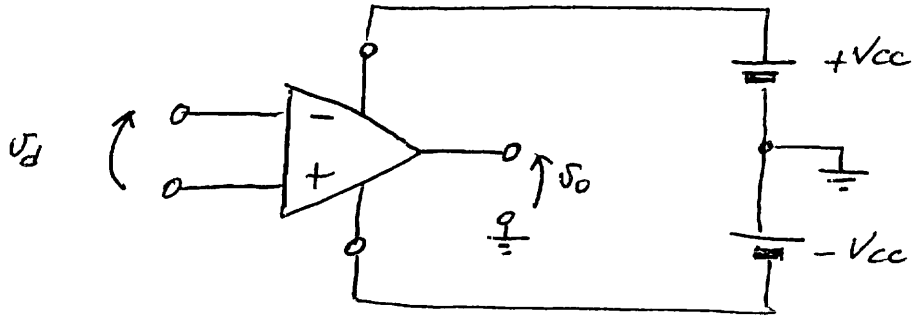
OPERATIONAL AMPLIFIER

The Operational amplifier is the most extensively used analog IC. The Op Amp. main reasons of popularity are its versatility and the fact that has characteristic that closely approach the ideal.
Besides its quite easy to design circuits using the op amp as building block.

- VERSATILITY
- CLOSE TO IDEAL
- EASY TO USE



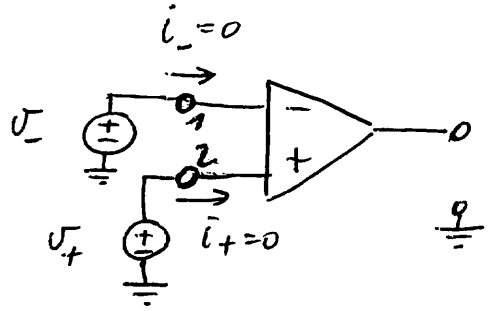
$$-v_d = v_+ - v_-$$

We will look at the op amp as a black box that can be used as a circuit building block without worrying about what is inside it. → We will study only its terminal characteristics and its applications.

An op amp is a rather complex circuit which is made up of a large number of transistors.

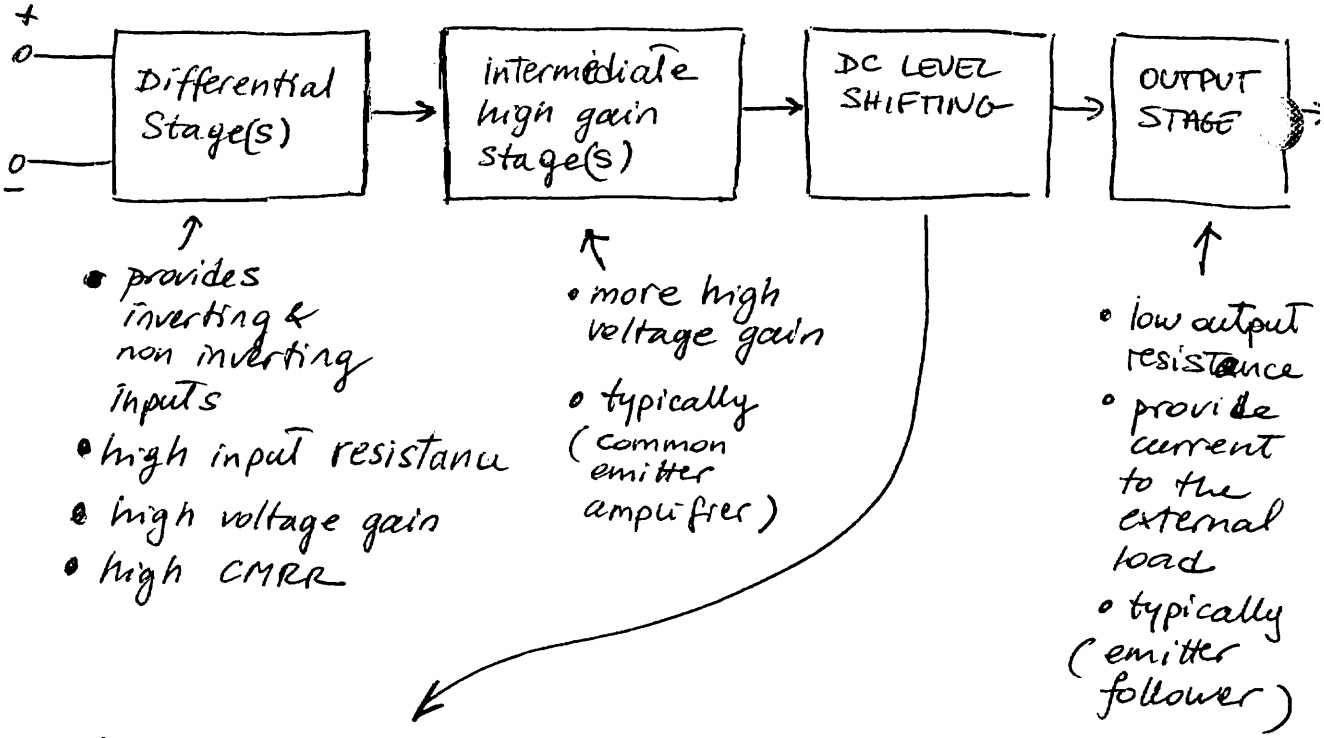
The name OPERATIONAL Amplifier from one of the original uses of the op amps to perform mathematical operations in analog computers

Op Amp → is a 2-input voltage-controlled voltage source whose output voltage is proportional to the difference between the two input voltages



Terminal 1: is called INVERTING input terminal
Terminal 2: is called NON INVERTING input terminal

Inside the op Amp architecture is as follow:



since no coupling capacitors can be used (~~the op~~ amp. has to operate ~~down to dc~~)
it maybe necessary shift the quiescient voltage of one stage before applying its output to the following stage.
level shifting is also required in order for the output to be close to 0 in the quiescient state.
(the level shifter R_i should be high and the R_o low)

IDEAL OP AMP

$R_i = \infty$ → the current is $\emptyset$

Bandwidth $= \infty$ → (direct coupled = dc amplifier)

$R_o = 0$

$A_d = \infty$ differential gain (open loop gain)

$A_c = 0$

→ no much sense to take an op amp and use it alone (= open loop configuration)

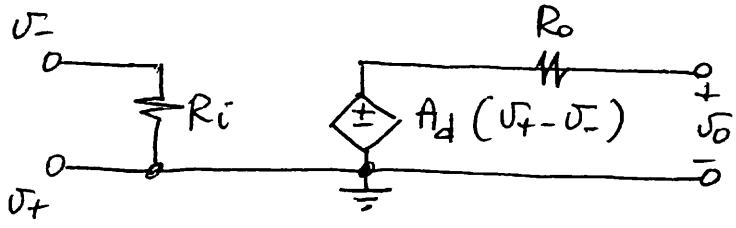
the op amp responds only to the difference signal $v_d = v_+ - v_-$ and hence ignores any signal common to both inputs

⇕

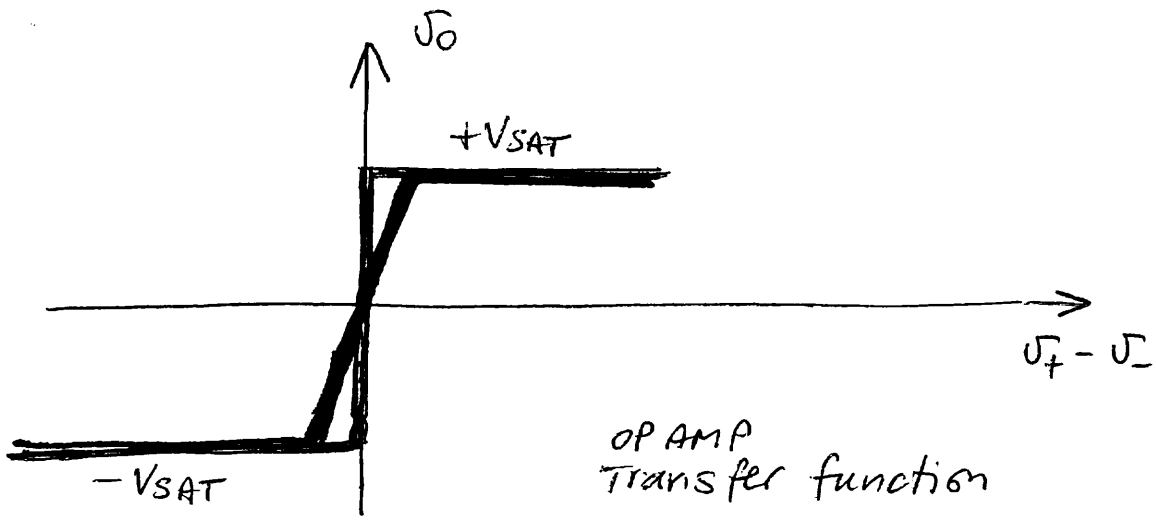
$v_o = 0$ when $v_+ = v_-$

(this property is called common mode rejection ratio)

$A_c = 0 \leftrightarrow CMRR = \infty$



Equivalent circuit of op amp.



OP AMP
Transfer function

The op. amp in open-loop is of very little use!

↝ we need to build some network around it (closed loop)

↓

Feedback

typical op amp numbers:

$A_d = 50000$

$I_{OUT_{max}} = 50\ mA$

$R_i = \begin{cases} 10\ M\Omega & BJT \\ 10^{12}\ \Omega & FET \end{cases}$

$CMRR = 100\ dB$

offset voltage = 1 mV

offset current = 10 nA

offset drift = 0.1 mV/°C

THE INVERTING AMPLIFIER

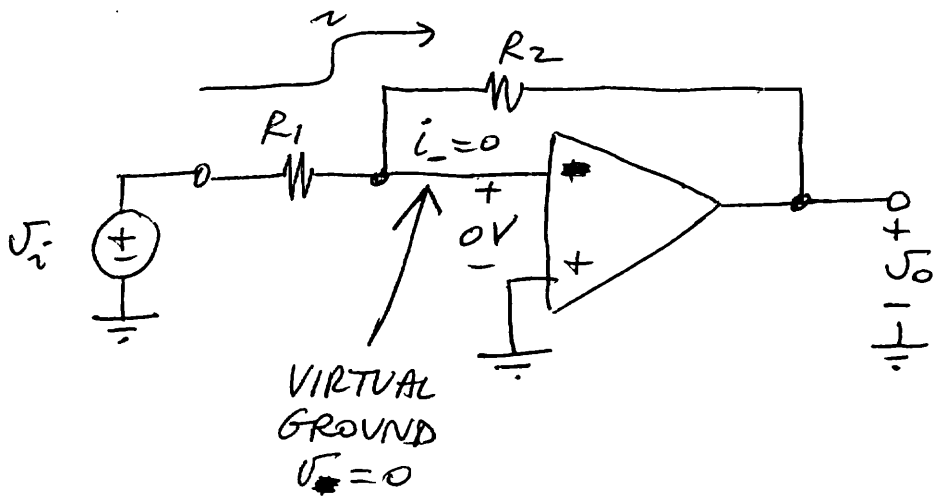
We want to build a circuit that produces a finite output voltage v_o.
Then the voltage between the op amp input terminals should be negligibly small:

$$v_o = \underbrace{A_d}_{\downarrow \infty} \underbrace{(v_+ - v_-)}_{\downarrow 0}$$

To keep $(v_+ - v_-) = 0$ it means that the two input terminals must be tracking each other in potential at all time: $v_+ \approx v_-$

↓

A VIRTUAL short circuit exists between the two terminals !!



(since v_+ is physically at ground)

$$v_i = R_1 \cdot i$$

$$v_o = -R_2 \cdot i$$

$$\Rightarrow \boxed{\frac{v_o}{v_i} = -\frac{R_2}{R_1}}$$

↑ voltage Amplification

- Input Resistance

$$R_i = \frac{v_i}{i} = R_1 \longrightarrow$$

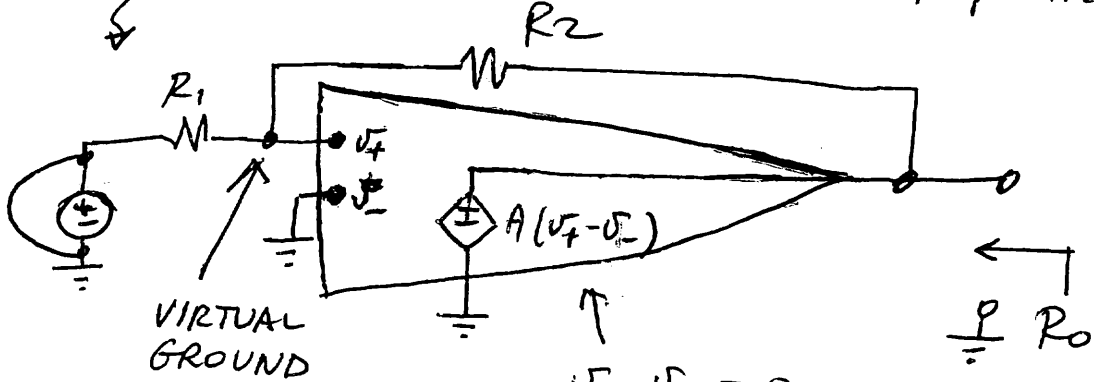
To make R_i high we must choose R_1 high

↓

which means an even higher R_2 if we want to achieve high voltage ampl.

→ This could become impratical!

- Output Resistance



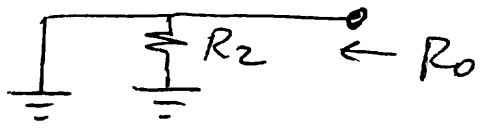
$v_+ - v_- = 0$

Therefore the controlled voltage is a short circuit

A_V, R_i, R_o

dependent only upon values of the external circuit elements

$$\boxed{R_o = 0}$$



If the open loop gain is finite the analysis become more complicated !!

$$\begin{cases} v_i = R_1 \cdot \hat{i} + R_2 \cdot \hat{i} + v_o \quad \Rightarrow \\ v_i = R_1 \cdot \hat{i} + v_- - v_+ \rightarrow v_i = R_1 v_i - (v_+ - v_-) \\ v_o = A_d (v_+ - v_-) \end{cases}$$

$$\Downarrow$$

$$\begin{cases} v_i = (R_1 + R_2)\hat{i} + v_o \\ v_+ - v_- = \dfrac{v_o}{A_d} \\ v_i = R_1 \cdot \hat{i} - \dfrac{v_o}{A_d} \end{cases} \Rightarrow \hat{i} = \frac{v_i + v_o/A_d}{R_1}$$

$$v_i = (R_1+R_2)\frac{v_i}{R_1} + \frac{(R_1+R_2)}{R_1} v_o/A_d + v_o$$

$$v_i \left(1 - \frac{R_1+R_2}{R_1}\right) = v_o \left(1 + \frac{R_1+R_2}{R_1 A_d}\right)$$

$$v_i \left(-\frac{R_2}{R_1}\right) = v_o \left(1 + \frac{R_1+R_2}{R_1} \cdot \frac{1}{A_d}\right)$$

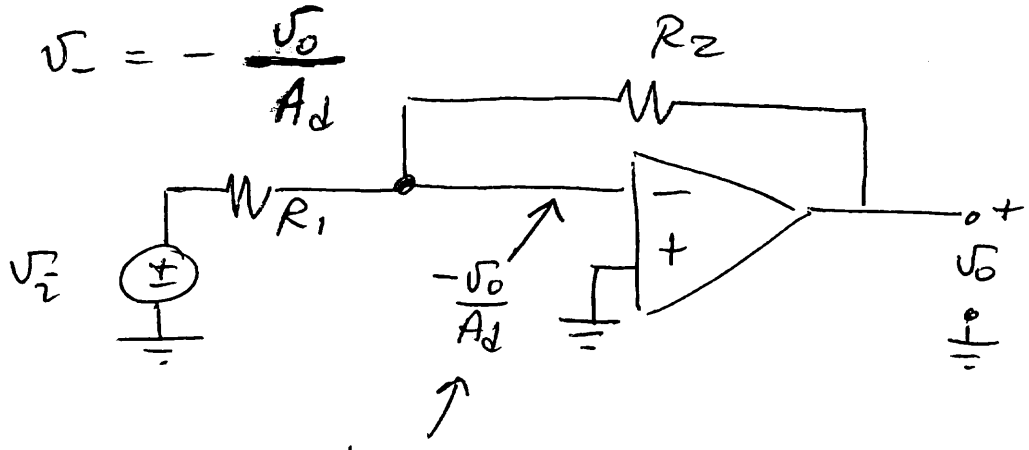
$$\frac{v_o}{v_i} = \frac{-R_2/R_1}{1 + \frac{1}{A_d}(1 + R_2/R_1)} \xrightarrow[A_d \to \infty]{} -R_2/R_1$$

$$\Downarrow$$

more pratically is enough to have

$$A_d \gg 1 + R_2/R_1$$

The value of A_d has an effect on the value of the **max voltage gain that I can achieve** with my designed amplifier !!



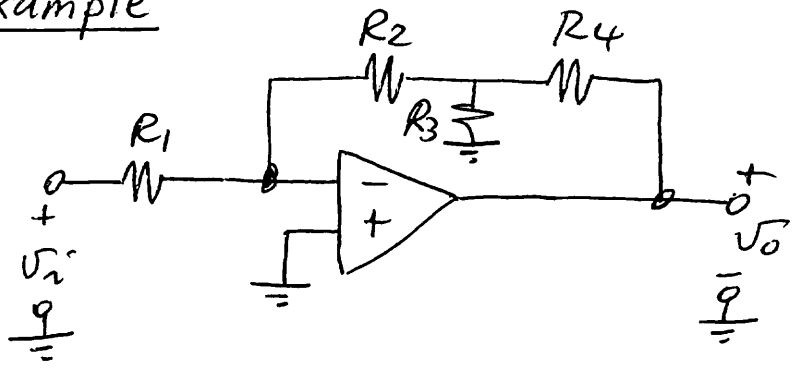
it tells how good is the VIRTUAL GROUND ASSUMPTION !!

The external element R2 is used to feed back a portion of the output signal to the input.
Since the feedback element is placed between the output and the inverting input a portion of the output subtracts from the input !

↓

NEGATIVE FEEDBACK

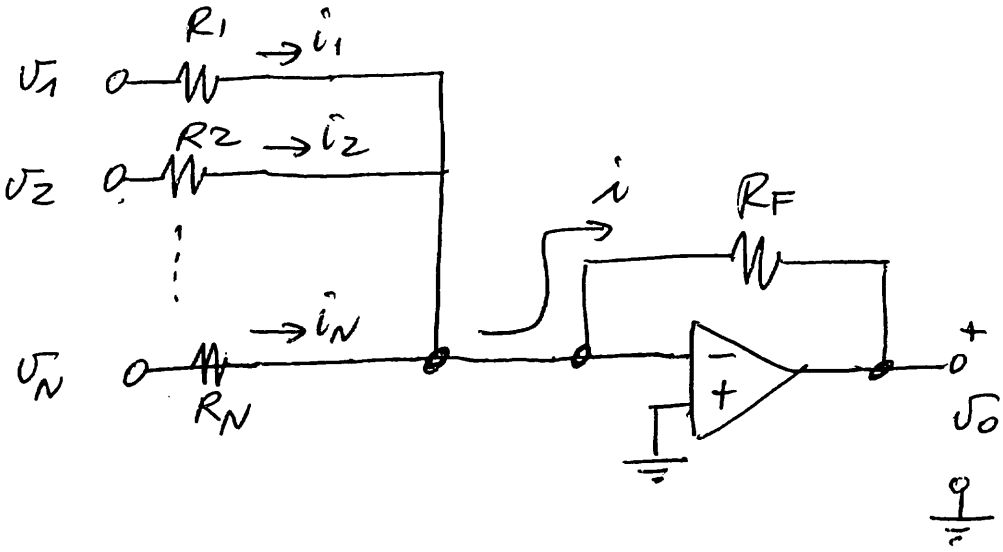
Example



$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}\left(1 + \frac{R_4}{R_2} + \frac{R_4}{R_3}\right)$$

I can keep R_1 high so that R_i is high and play with R_4/R_2 and R_4/R_3 to get an high voltage gain.

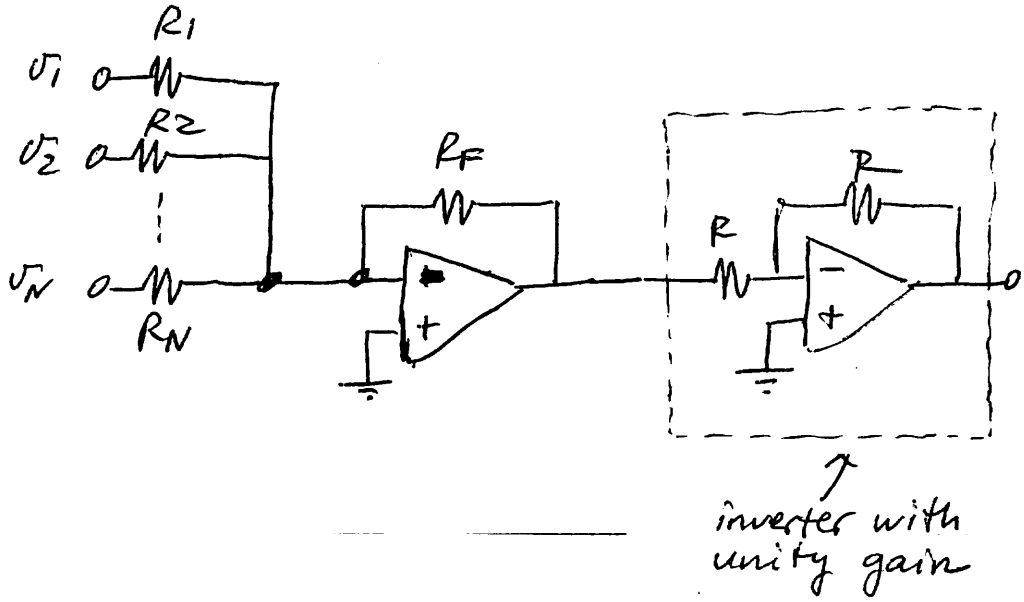
The WEIGHTED INVERTING ADDER



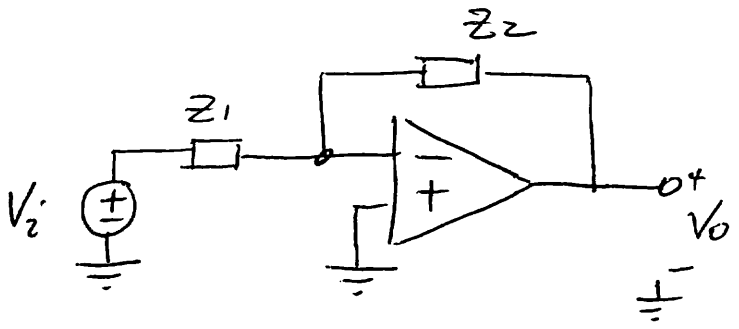
$$i = i_1 + i_2 + \dots + i_N = \frac{v_1}{R_1} + \frac{v_2}{R_2} + \dots + \frac{v_N}{R_N}$$

$$v_o = -iR_F = -\left(\frac{R_F}{R_1}v_1 + \frac{R_F}{R_2}v_2 + \dots + \frac{R_F}{R_N}v_N\right)$$

WEIGTHED NON INVERTING ADDER

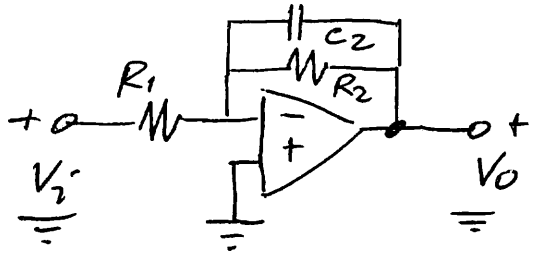


INVERTING FILTERS (ACTIVE)



$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)}$$

LOW PASS ACTIVE FILTER (of first order)

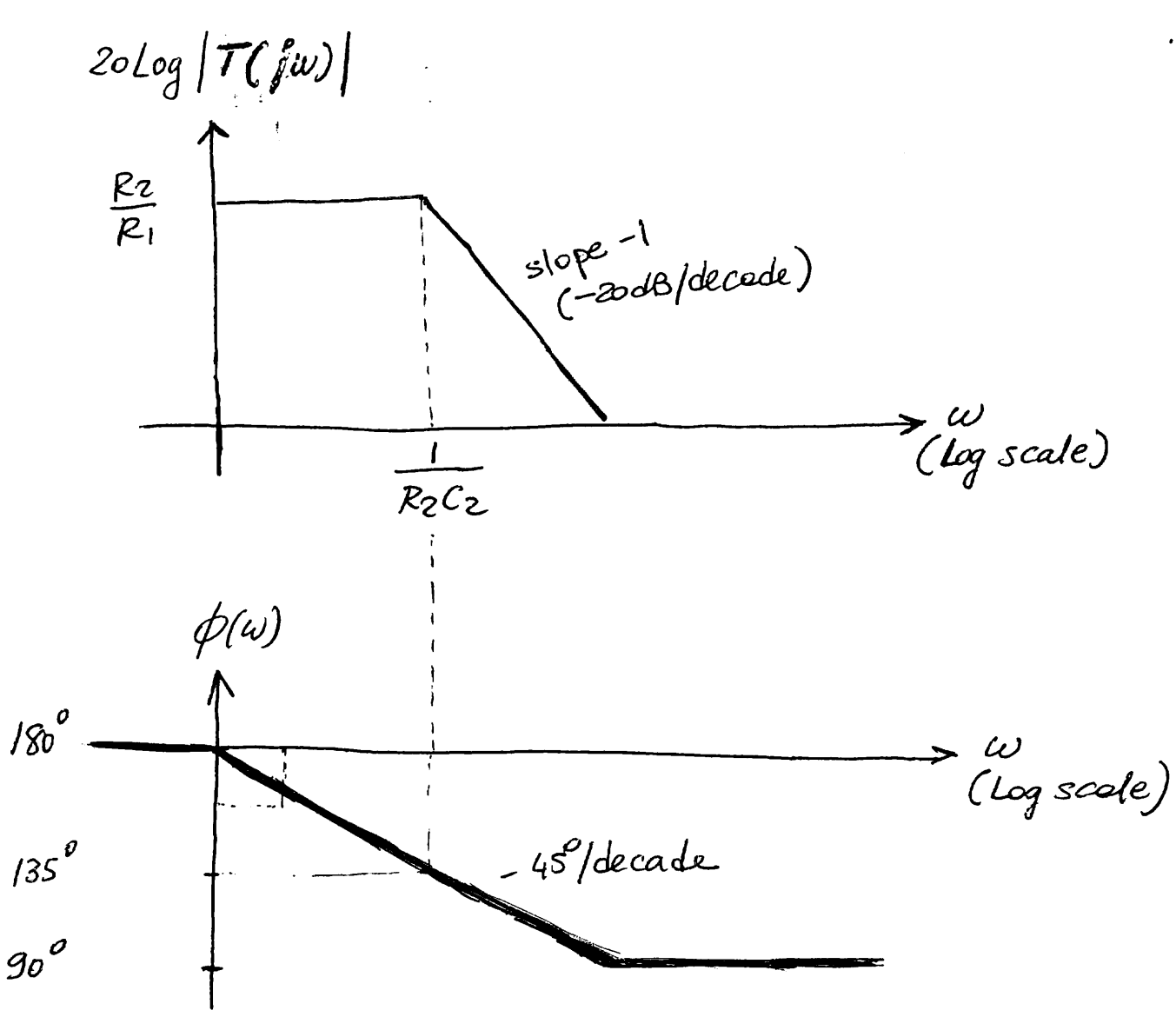


$$Z_1 = R_1$$

$$Z_2 = \frac{R_2 \cdot 1/sC_2}{R_2 + 1/sC_2} = \frac{R_2}{sR_2C_2 + 1}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + sR_2C_2} = T(s)$$

$$T(j\omega) = \frac{-R_2/R_1}{1 + j\omega R_2C_2}$$



Example

design the circuit to obtain a dc gain of 40dB, a 3-dB frequency of 1kHz, an input resistance of 1 kΩ

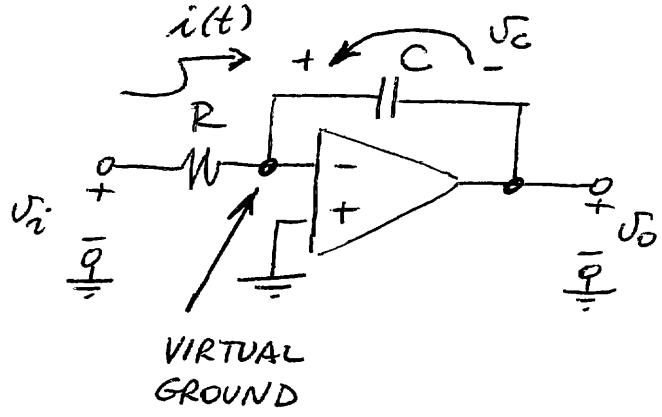
At what frequency does $|T(j\omega)|$ become 1? what is $\phi(\omega)$ at this frequency?

$R_2/R_1 = 100$ $\quad \underbrace{R_1 = 1\,k\Omega}_{\parallel\ R_i} \rightarrow R_2 = 100\,k\Omega$ $\quad 2\pi f_0 = \frac{1}{R_2 C_2} \Rightarrow C_2 = 1.59\,nF$

it takes 2 decades to fall from 40dB to 0dB ($\equiv |T|=1$) $\Rightarrow f_0 \cdot 10^2$

since $f_0 \cdot 100 >> f_0 \Rightarrow \phi(f_0 \cdot 100) \approx 90°$

Miller integrator (IDEAL INTEGRATOR) 3.6



LOW PASS FILTER

$$v_o(t) = -v_c(t)$$

$$i(t) = C\frac{dv_c}{dt} \rightarrow i(t) = -C\frac{dv_o}{dt}$$

$$v_i(t) = R \cdot i \rightarrow v_i(t) = -RC\frac{dv_o}{dt}$$

$$v_o(t) = -\frac{1}{RC}\int_0^t v_i(t)\,dt$$

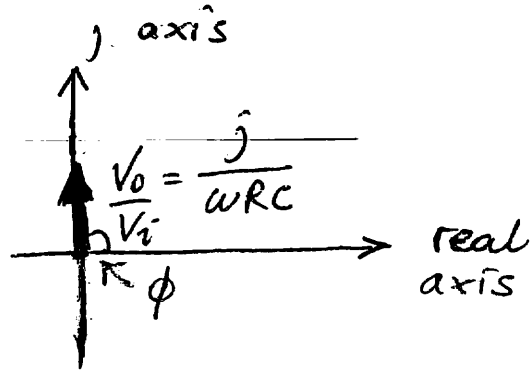
In the frequency domain:

$$V_i(s) = -RCsV_o(s)$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{sRC}$$

$$s = j\omega$$

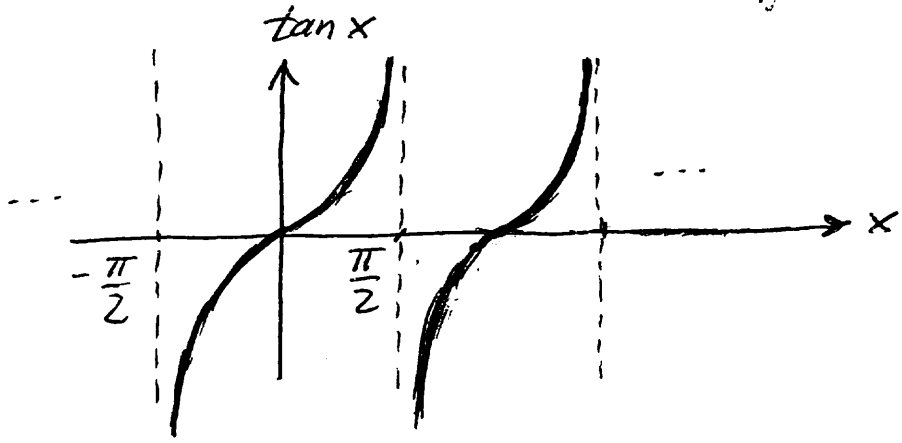
$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega RC}$$

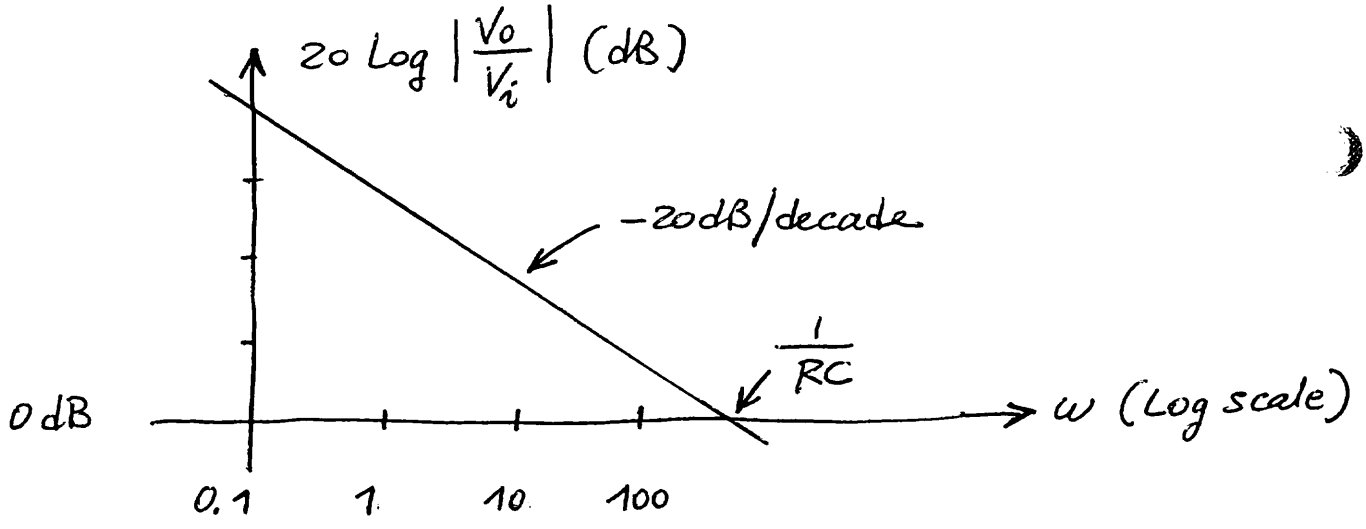


$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\omega RC}$$

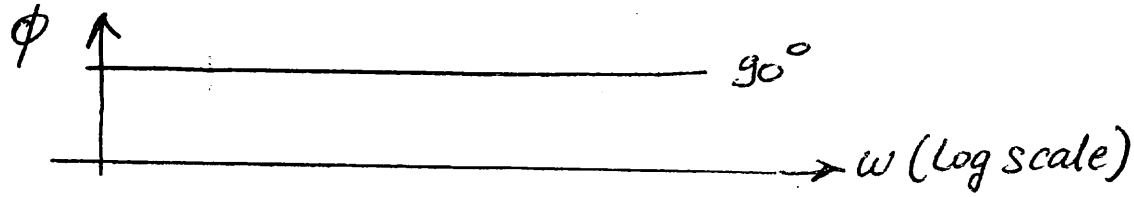
$$\phi = +90^\circ = \arctan \frac{1/\omega RC}{0}$$

(1/ωRC: imaginary part; 0: real part)





As ω increases by a decade the magnitude decrease by 20 dB ($20 \text{Log} \frac{1}{10} = -20$ dB). Therefore the Bode plot of the integrator magnitude is a straigth line of slope -20 dB/decade



The Line intercept the 0 dB line at the frequency that makes

$$\left|\frac{V_o}{V_i}\right| = 1 \rightarrow \frac{1}{\omega_o RC} = 1 \rightarrow \omega_o = \frac{1}{RC}$$

$$\downarrow$$

$$20 \text{ Log} \left|\frac{V_o}{V_i}\right| = 0 \text{ dB}$$

$$= 1$$

If we look more closely at this circuit, we see that unfortunately it will give us a lot of troubles !!

For $\omega = 0$ (at dc) the integrator transfer function is infinite $\frac{1}{\omega RC} \xrightarrow[\omega \to 0]{} \infty \Rightarrow$ this indicates that the op. amp is operating in open loop !

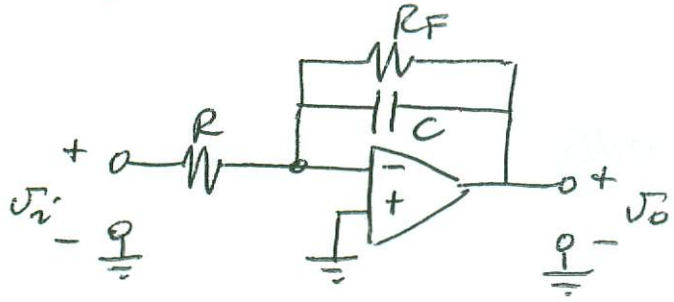
$$\downarrow$$

That's no big surprise ! $\rightarrow$ since the feedback element is a capacitor and at dc the capacitor behaves as an open circuit $\Rightarrow$ then there is no negative feedback. $\Rightarrow$

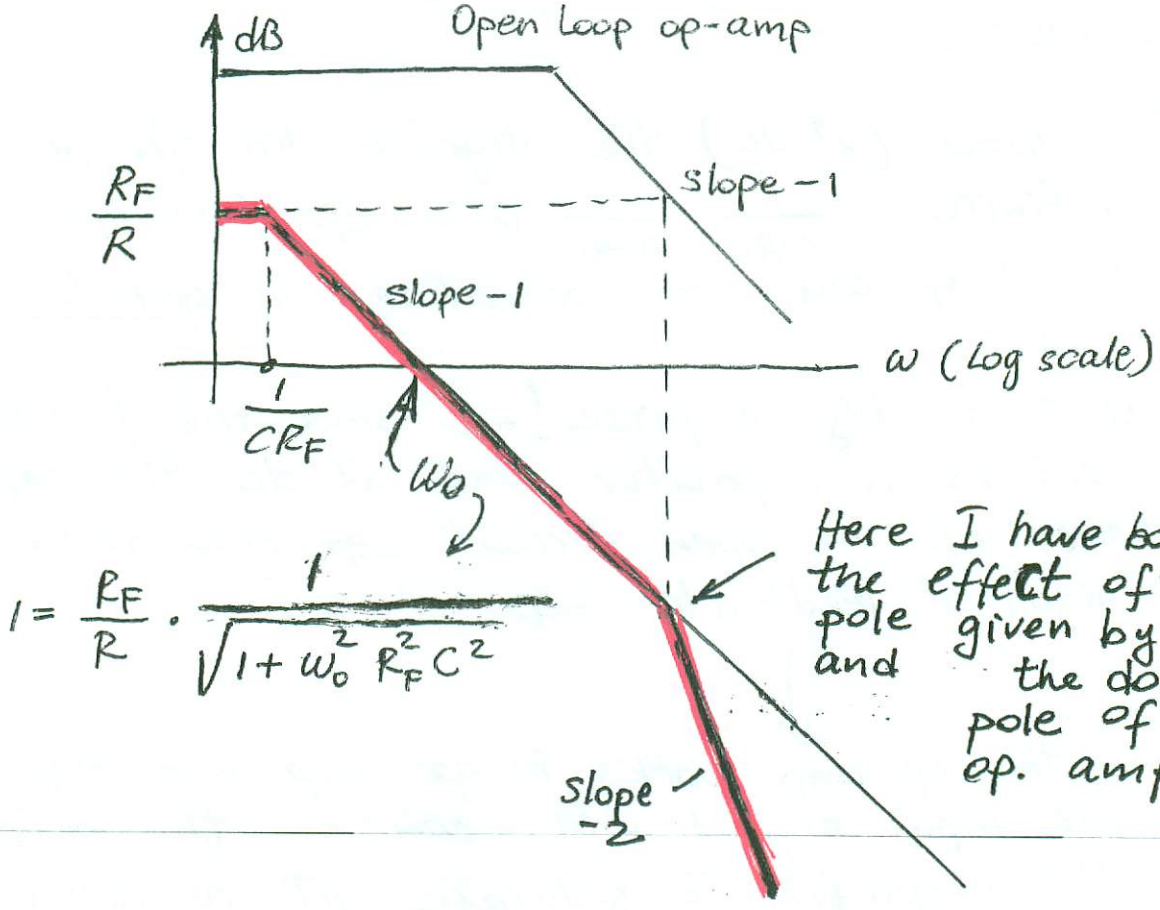
$$\downarrow$$

since the op amp works in open loop any tiny dc in the input signal will cause the output of the amplifier to saturate at a voltage close to $+V_{cc}$ or $-V_{cc}$ depending on the polarity of the input dc signal.

The solution is to connect a very big R_F in parallel with the capacitor
The resistor R_F closes the feedback loop at dc
→ unfortunately the resulting integrator is no longer ideal



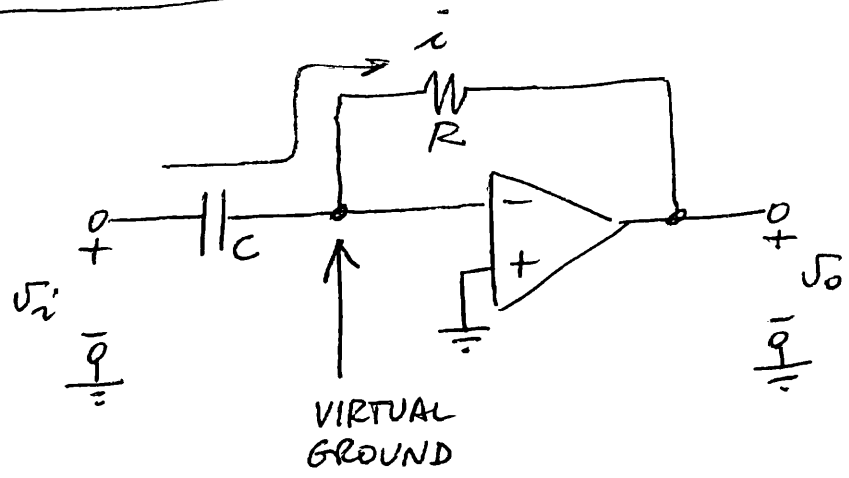
$$\frac{V_o}{V_i} = -\frac{R_F}{R} \cdot \frac{1}{1+sCR_F}$$



$$1 = \frac{R_F}{R} \cdot \frac{1}{\sqrt{1+\omega_0^2 R_F^2 C^2}}$$

DIFFERENTIATOR

HIGH PASS FILTER



$$v_i(t) = v_c(t) \rightarrow i(t) = C\frac{dv_c(t)}{dt} = C\frac{dv_i(t)}{dt}$$

$$v_o = -R \cdot i$$

$$\downarrow$$

$$v_o(t) = -RC\frac{dv_i(t)}{dt}$$

In the frequency domain:

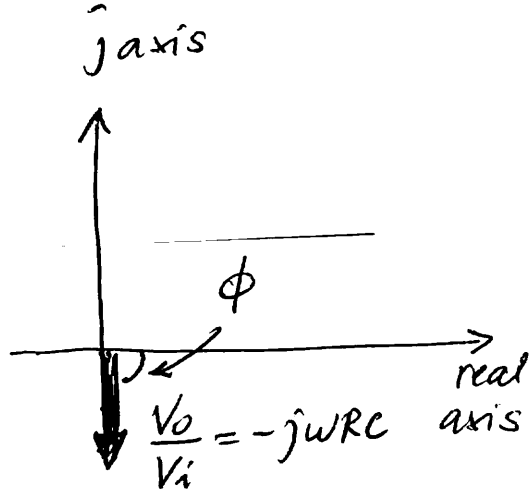
$$V_o(s) = -RCs\,V_i(s)$$

$$\downarrow$$

$$\frac{V_o(s)}{V_i(s)} = -sRC$$

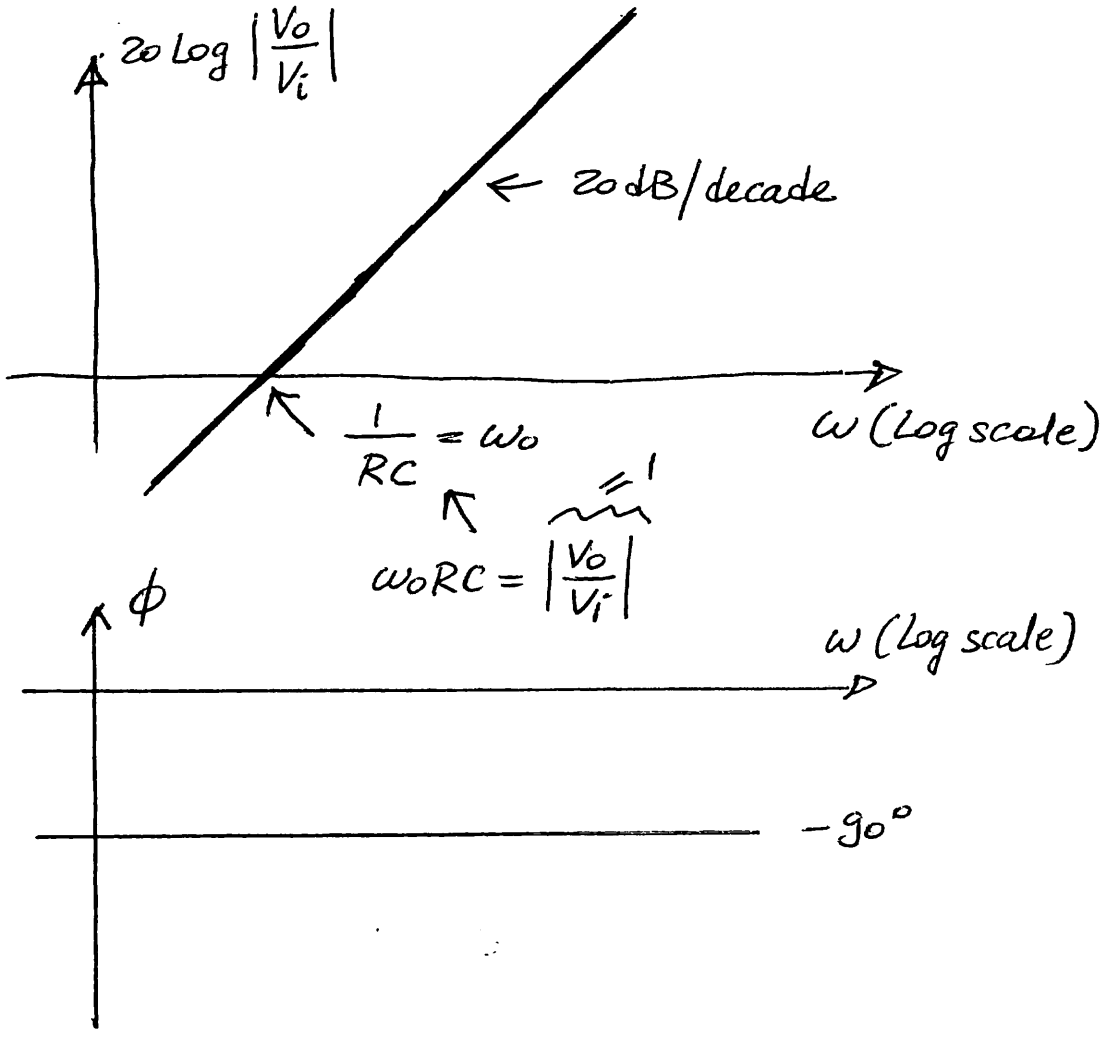
$$\downarrow s = j\omega$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega RC$$



$$\left|\frac{V_o}{V_i}\right| = \omega RC$$

$$\phi = -90^\circ$$



If we think a little more about this circuit we see that is problematic!
Every time there is sharp change in $v_i(t)$ a spike is introduced at the output
→ sudden changes are typical of a picked-up interference → in this case the differentiator circuit is a "noise" magnificator.
Another (even bigger issue is that it suffer from stability problems

for $v_i(t) = u(t)$ ← unity step function

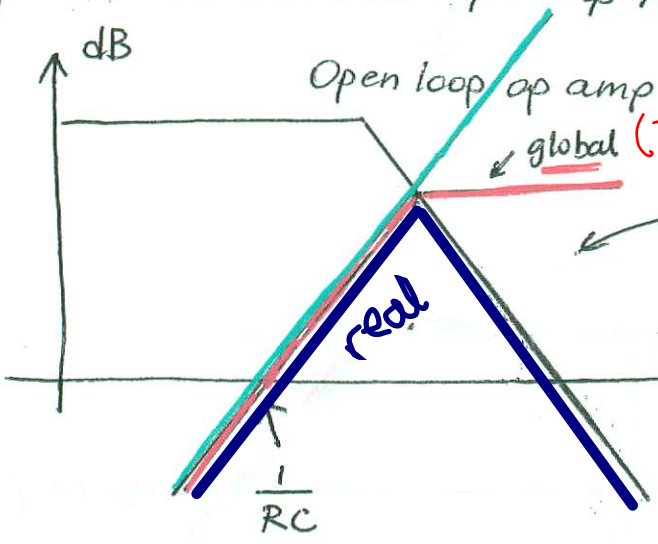
$$\downarrow$$

$$v_o(t) = -RC \frac{du(t)}{dt}$$

$$\downarrow$$

$$v_o(t) = -RC\,\delta(t)$$ ← Dirac impulse function

Keeping into account the op-amp response we can have:

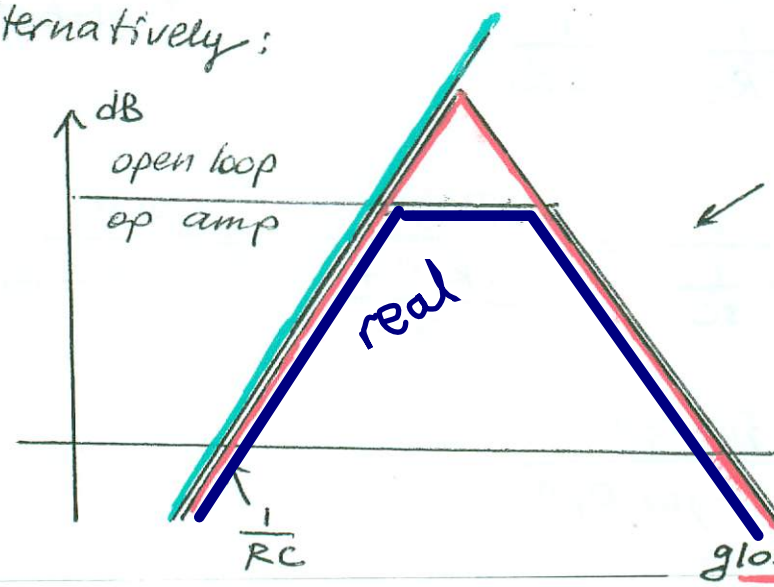


(theoretical)

In this case at the high frequency the ampl. decrease dramatically !!

which is the opposite of what a differentiator (high pass filter) is supposed to do !

or alternatively:



In this case after a while the op-amp works in open loop with the well known problems !

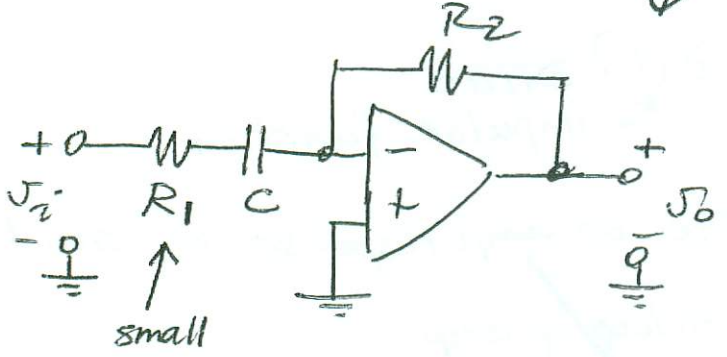
(theoretical)

The solution is to add a small resistance in series to the capacitance

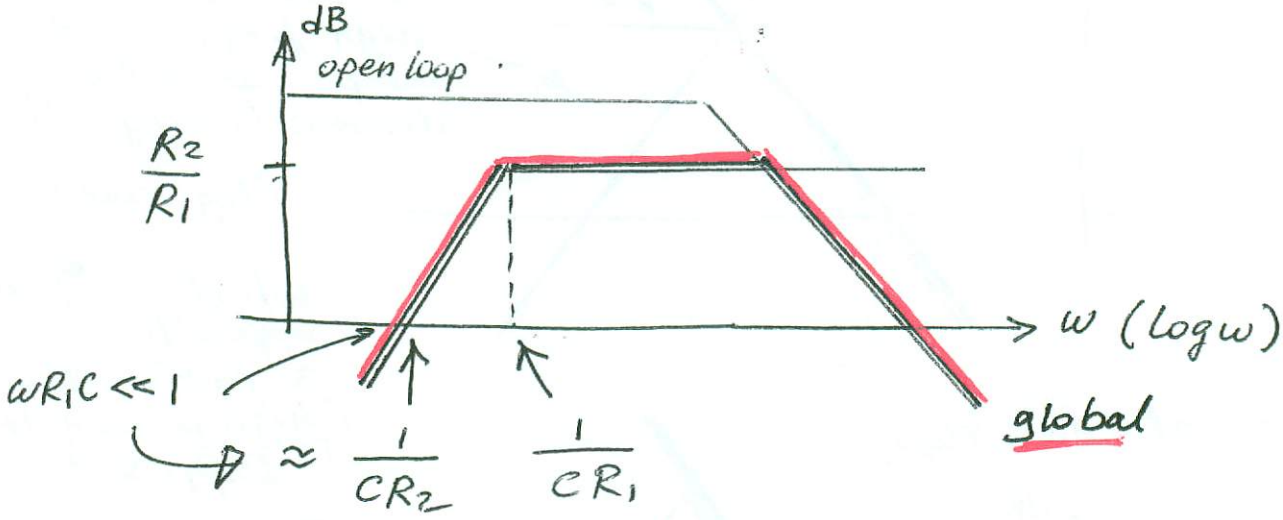
↓

unfortunately the circuit is no longer an ideal differentiator

↓



ACTIVE HIGH PASS FILTER (first order)



$$\frac{V_o}{V_i} = -\frac{R_2}{R_1 + \frac{1}{sC}} = -\frac{R_2}{\frac{sR_1C+1}{sC}} = -\frac{sR_2C}{1+sR_1C}$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{j\omega R_2 C}{1+j\omega R_1 C}$$

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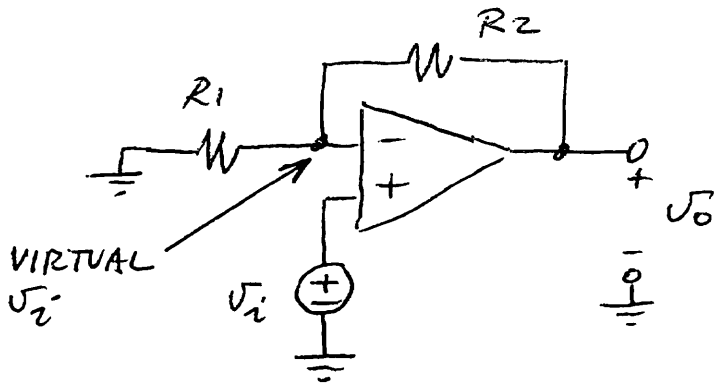
asimptotic analysis:

$\omega R_1 C \gg 1 \longrightarrow V_o/V_i \approx \frac{-j\omega R_2 C}{j\omega R_1 C} = -R_2/R_1$

$\omega R_1 C \ll 1 \longrightarrow V_o/V_i \approx j\omega R_2 C$

NON INVERTING AMPLIFIER



To produce a finite output voltage v_o the voltage between the op amp inputs must be negligible

$$v_o = A_d (v_+ - v_-)$$

$A_d \to \infty$, $(v_+ - v_-) \to 0$

Therefore:

$$v_o = R_2 \cdot i + v_i^-$$

$$v_i^- = R_1 \cdot i \longrightarrow i = \frac{v_i^-}{R_1}$$

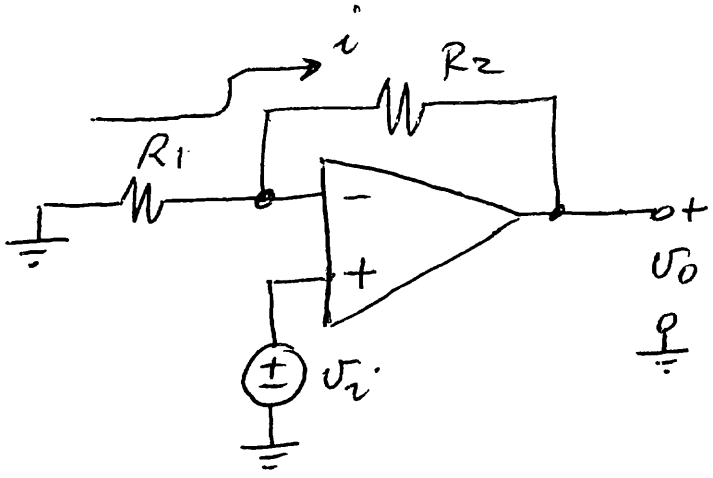
$$\downarrow$$

$$v_o = R_2 \cdot \frac{v_i^-}{R_1} + v_i^- = \left(\frac{R_2}{R_1} + 1\right) v_i^-$$

$$\downarrow$$

$$\frac{v_o}{v_i^-} = 1 + \frac{R_2}{R_1}$$

Let's see what is the effect of the finite open loop gain:



$$v_o = A_d \cdot (v_+ - v_-)$$

$v_+ = v_i$ $\qquad$ $v_- = R_2 i + v_o$

$$v_- = -R_1 \cdot i \Rightarrow i = -\frac{v_-}{R_1}$$

$$v_- = -R_2 \frac{v_-}{R_1} + v_o \rightarrow v_-\left(1 + \frac{R_2}{R_1}\right) = v_o$$

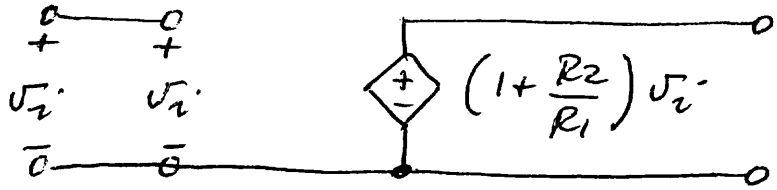
$$v_- = \frac{v_o}{1 + \frac{R_2}{R_1}}$$

$$v_o = A_d v_+ - A_d v_- = A_d v_i - A_d \frac{v_o}{1 + \frac{R_2}{R_1}}$$

$$v_o\left(1 + \frac{A_d}{1 + R_2/R_1}\right) = A_d \cdot v_i$$

$$\frac{v_o}{v_i} = \frac{A_d}{1 + \frac{A_d}{1 + R_2/R_1}} = \frac{A_d(1 + R_2/R_1)}{1 + \frac{R_2}{R_1} + A_d} =$$

$$\frac{v_o}{v_i} = \frac{1 + R_2/R_1}{\dfrac{1 + R_2/R_1 + A_d}{A_d}} \xrightarrow{A_d \gg 1 + \frac{R_2}{R_1}} 1 + \frac{R_2}{R_1}$$



Equivalent circuit

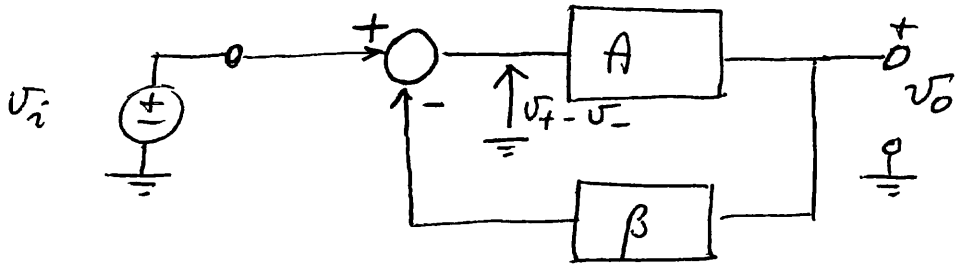
- Input Resistance

$$R_i = \frac{v_i}{i} = \infty$$

- Output Resistance

$$R_o = 0$$

FEEDBACK PERSPECTIVE:



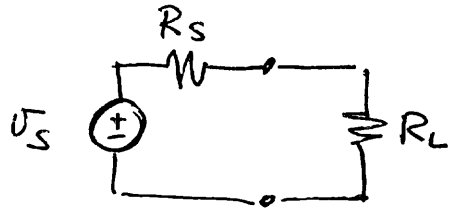
$$\left.\begin{aligned} v_- &= \beta v_o \\ v_+ &= v_i \\ v_o &= A \cdot (v_+ - v_-) \end{aligned}\right\} \rightarrow \frac{v_o}{v_i} = \frac{A}{1 + \beta A} \xrightarrow{\beta A \gg 1} \frac{1}{\beta}$$

closed loop

For A big the gain depends only on the feedback network

VOLTAGE FOLLOWER

There are situation where I may have to connect a source with a high impedance to a low impedance load

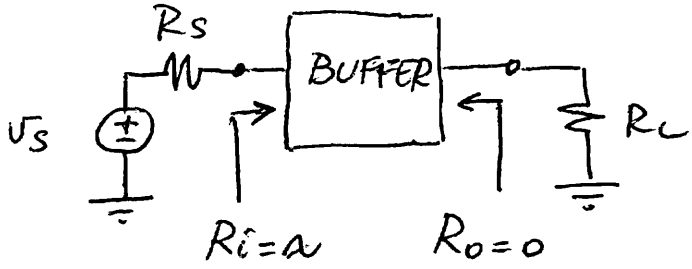


since $R_L \ll R_S$

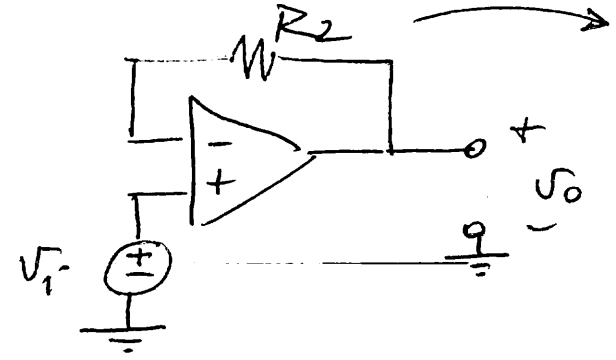
$$V_L = \frac{V_S}{R_L + R_S} R_L$$

most of the voltage from the source is dropped !!

It would be nice to have a circuit that is able to "buffer" source and load



Such a buffer is not required to provide any voltage gain → the output voltage must simply <u>follow</u> the input voltage and $R_i = \infty$ and $R_o = 0$

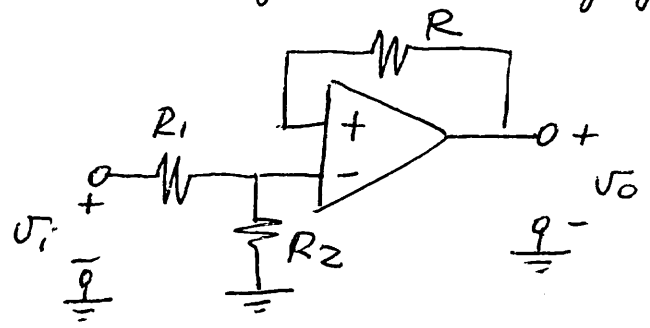


since no current flow through R2 I can put a short in place of R2

I can think of it as a non inverting amplifier where I put $R_1 \to \infty$ ($\frac{V_o}{V_i} = 1 + R_2/R_1$)

MORE OP-AMP CIRCUITS

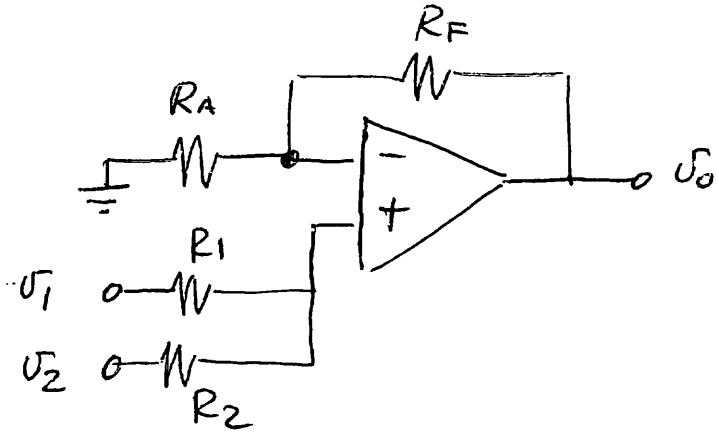
- Less than unity non inverting gain



$$\frac{V_o}{V_-} = 1$$

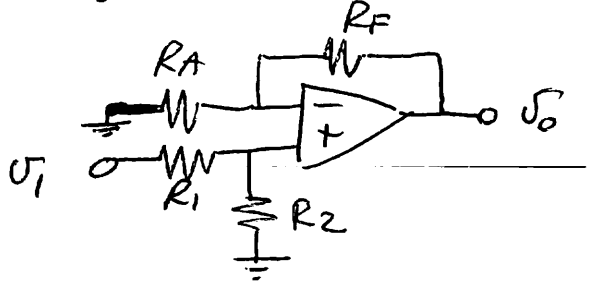
$$\frac{V_o}{V_i} = \frac{R_2}{R_1+R_2} \qquad V_- = \frac{V_i}{R_1+R_2} \cdot R_2$$

- NON INVERTING ADDER



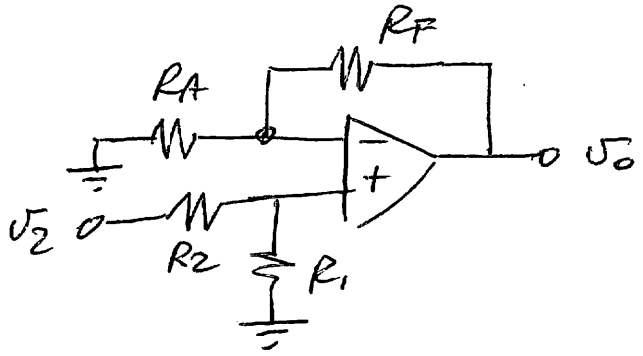
I apply superposition:

(1)



$$V_o' = \left(1 + \frac{R_F}{R_A}\right) \cdot \frac{R_2}{R_1+R_2} \; V_1$$

(2)

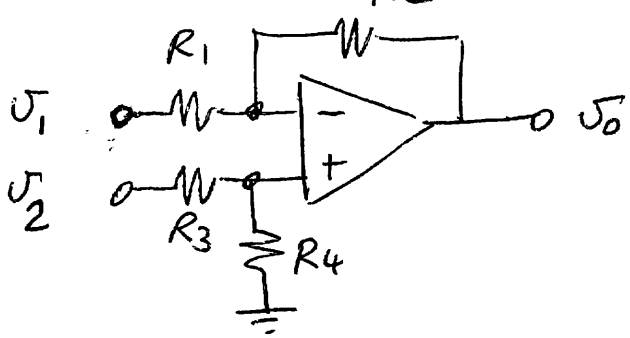


$$v_o'' = \left(1 + \frac{R_F}{R_A}\right) \cdot \frac{v_2}{R_2 + R_1} \cdot R_1$$

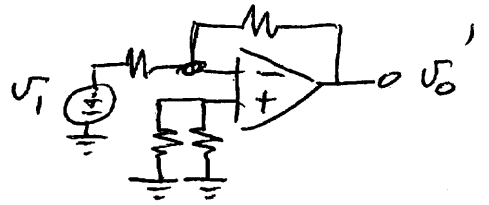
putting together;

$$v_o = v_o' + v_o'' = \left(1 + \frac{R_F}{R_A}\right)\left[\frac{R_2}{R_1+R_2} \cdot v_1 + \frac{R_1}{R_1+R_2} v_2\right]$$

- SUBTRACTOR (DIFFERENCE AMPLIFIER)
(Mixed Configuration)

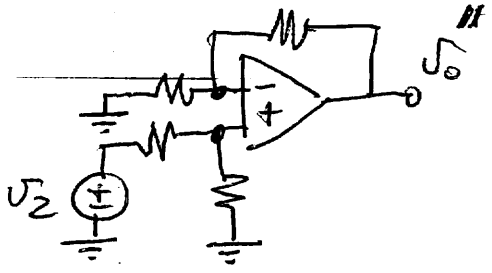


superposition



(1) $$v_o' = -\frac{R_2}{R_1} v_1$$

(2) $$v_o'' = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{v_2}{R_3 + R_4} \cdot R_4$$



putting together:

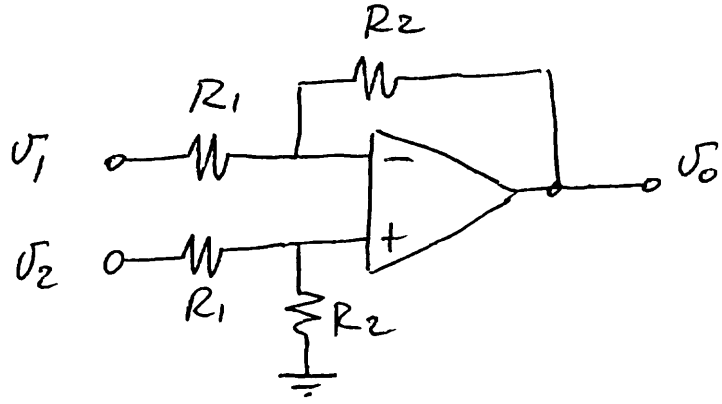
$$v_o = v_o' + v_o'' = -\frac{R_2}{R_1} v_1 + \frac{(1 + R_2/R_1)}{(1 + R_3/R_4)} v_2$$

If we want to make the weights balanced:

$$\frac{R_2}{R_1} = \frac{1 + R_2/R_1}{1 + R_3/R_4}$$

$$\Downarrow \quad R_4/R_3 = R_2/R_1 \quad \text{(let's try)} \quad \Leftrightarrow \quad \frac{R_3}{R_4} = \frac{1}{R_2/R_1}$$

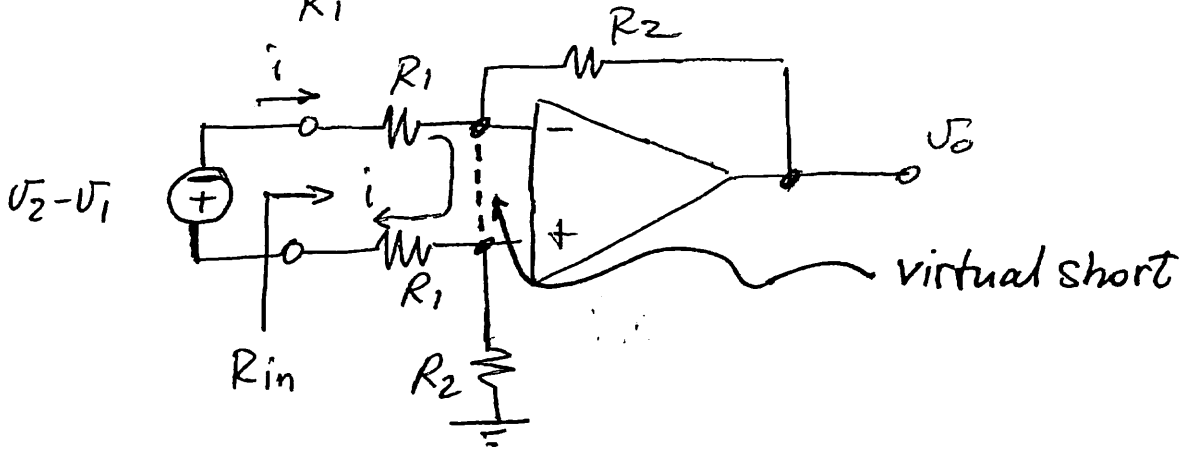
$$\frac{1 + R_2/R_1}{1 + \frac{1}{R_2/R_1}} = \frac{1 + R_2/R_1}{\frac{1 + R_2/R_1}{R_2/R_1}} \quad \rightarrow \quad = \frac{R_2}{R_1}$$



$$v_o = -\frac{R_2}{R_1}(v_1 - v_2)$$ ← This circuit amplify only differences

If a common signal is applied to both the inputs (e.g. a large picked-up interference from each of the long wires leading to the system) is REJECTED. !!

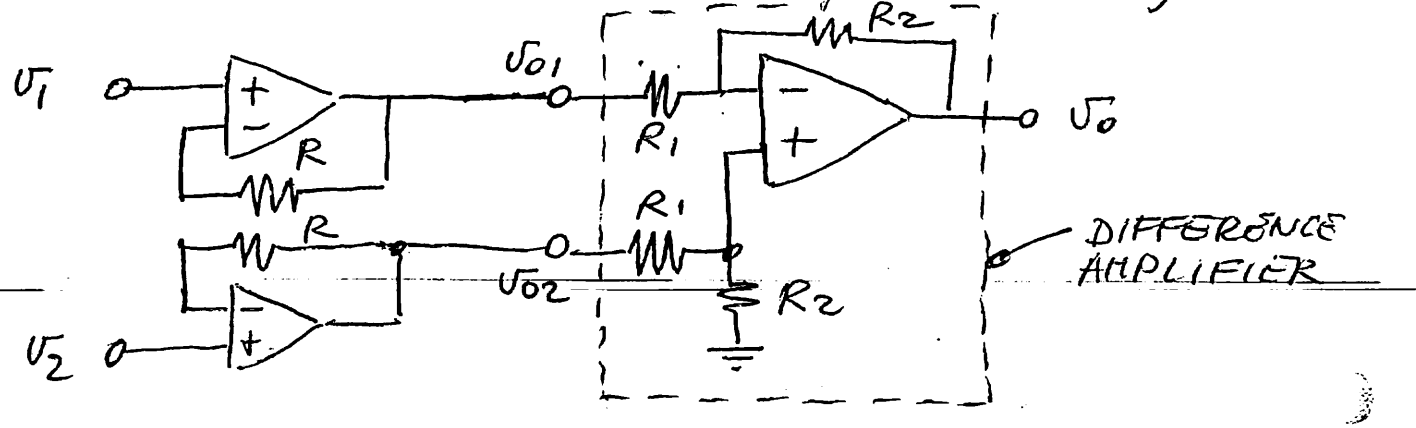
$$v_o = \frac{R_2}{R_1}(v_2 - v_1)$$



$$R_{in} = \frac{v_2 - v_1}{i} = R_1 \cdot i + 0 + R_1 \cdot i = 2 \cdot R_1$$

If the amplifier is required to have a large gain then R_1 will be relatively small and consequently the input resistance will be correspondingly small ↖ DRAWBACK !! small R_{in}

How can we solve this DRAWBACK ?
The easiest thing we can think of is to make use of buffers (voltage followers)

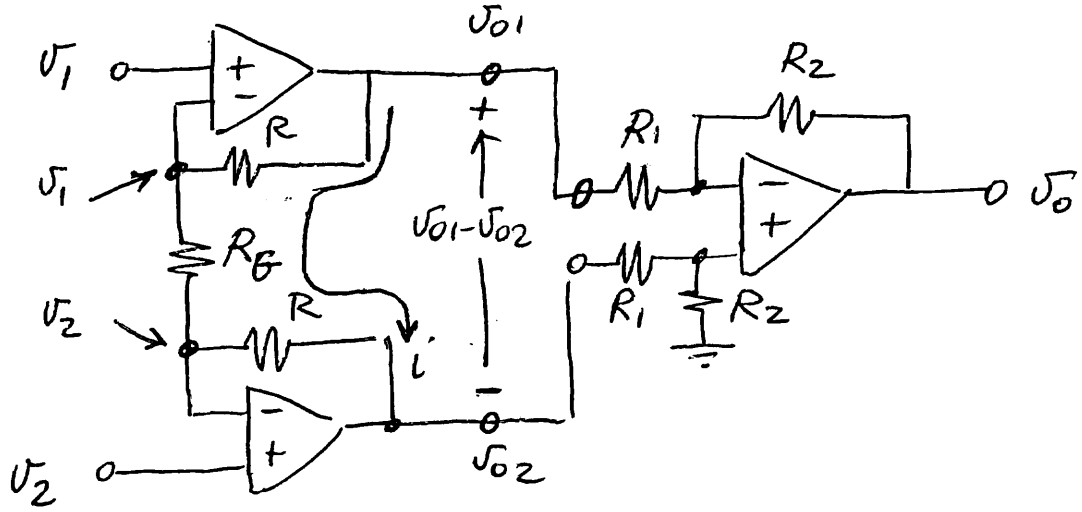


$$v_o = \frac{R_2}{R_1}(v_{o1} - v_{o2}) = \frac{R_2}{R_1}(v_1 - v_2)$$

This circuit solve already my problem, but actually it would be even nicer if I could be able to design a circuit that would allow me to make the gain adjustable.

To change the gain with the current circuit I have to either change R_1 or R_2 which means to touch 2 resistances at least. besides it's not a good idea to touch the difference amplifier → asymmetries in the R_2/R_1 ratios could cause troubles → once I built my difference amplifier and I verified it's perfect it's better to leave it alone !

I should focus on getting the gain out of the first stages.



$$v_{01}-v_{02} = R\cdot i + R_G\cdot i + R\cdot i \rightarrow v_{01}-v_{02} = 2R\cdot i + R_G\cdot i$$

$$i = \frac{v_1-v_2}{R_G} \qquad \uparrow\ v_1-v_2$$

↓

$$v_{o1} - v_{o2} = 2R \frac{v_1 - v_2}{R_G} + v_1 - v_2$$

$$\downarrow$$

$$v_{o1} - v_{o2} = (v_1 - v_2)\left(1 + \frac{2R}{R_G}\right)$$

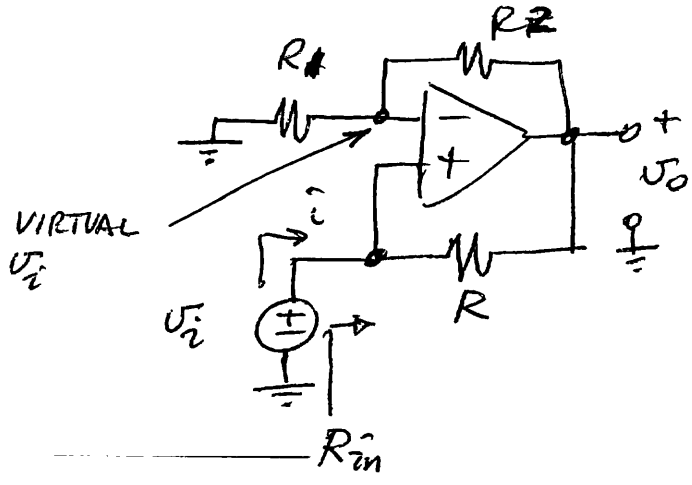
But we know as well that:

$$v_o = \frac{R_2}{R_1}(v_{o1} - v_{o2}) = \frac{R_2}{R_1}\left(1 + \frac{2R}{R_G}\right)(v_1 - v_2)$$

With this circuit I can adjust the gain just changing R_G !!!

This circuit is often called INSTRUMENTATION AMPLIFIER !

- NEGATIVE IMPEDANCE CIRCUIT



$$R_{in} = \frac{v_i}{i}$$

$$v_o = \left(1 + \frac{R_2}{R_1}\right) v_i'$$

$$i = \frac{v_i - v_o}{R} = \frac{v_i - (1 + R_2/R_1)\, v_i'}{R} = \frac{v_i'}{R}\left(1 - 1 - \frac{R_2}{R_1}\right)$$

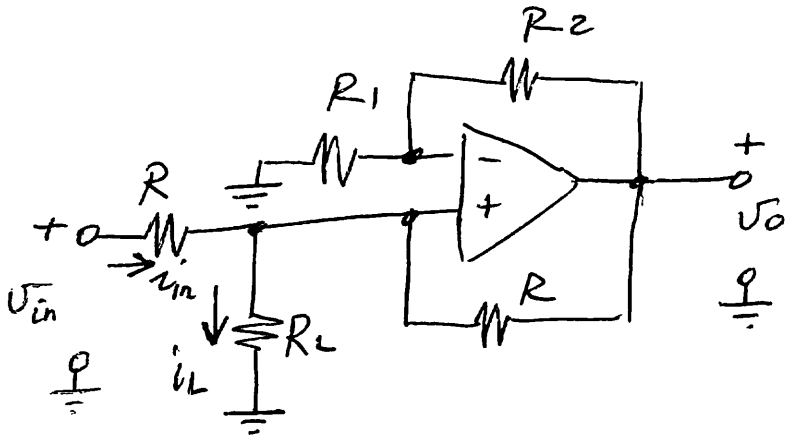
$$R_{in} = \frac{v_i'}{i} = -\frac{R R_1}{R_2}$$

- DEPENDENT CURRENT GENERATOR (VOLTAGE-TO-CURRENT CONVERTER)

This is a slight modification of the negative impedance circuit.

↓

produce a load current proportional to an applied voltage v_{in} and is independent of the load resistance



Let's make $R_1/R_2 = 1$

$$i_{in} = \frac{v_{in}}{R_{in}} = \frac{v_{in}}{R + \dfrac{R_L \cdot (-RR_1/R_2)}{R_L + (-RR_1/R_2)}} \quad \overset{R_1/R_2 = 1}{=}$$

$$= \frac{v_{in}}{R + \dfrac{R_L R}{R_L - R}}$$

We are interested in V_L and I_L !

$$v_L = v_{in} - R \cdot i_{in}$$

$$i_L = \frac{v_L}{R_L} = \frac{v_{in}}{R_L} - \frac{R \cdot v_{in}}{R - \frac{R_L R}{R_L - R}} \cdot \frac{1}{R_L} =$$

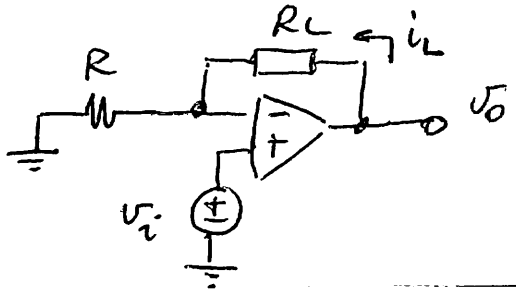
$$= \frac{v_{in}}{R_L} - \frac{R \cdot (R_L - R)\, v_{in}}{R \cdot R_L - R^2 - R R_L} \cdot \frac{1}{R_L}$$

$$= v_{in} \left(\frac{1}{R_L} + \frac{(R_L - R)}{R \cdot R_L} \right)$$

$$= v_{in} \frac{R + (R_L - R)}{R \cdot R_L} =$$

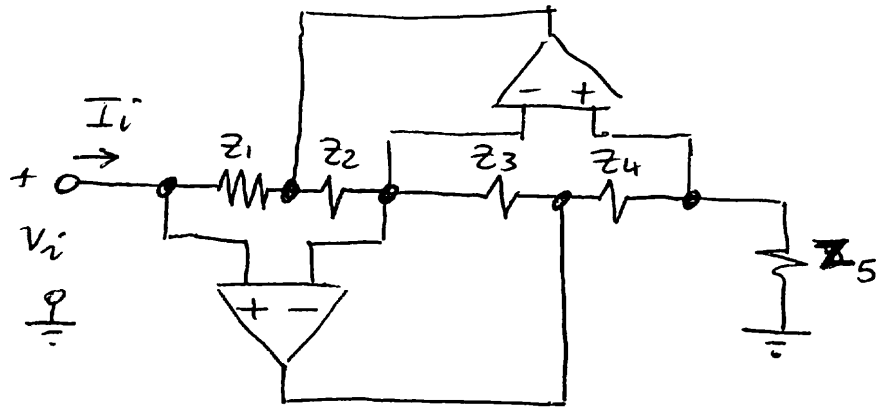
$$= \frac{v_{in}}{R}$$

In the case we can afford to have the load floating (neither side grounded) we can use an even simpler circuit (→ non inverting ampl. where R_2 is replaced by the load R_L)



$$i_L = -\frac{v_i}{R}$$

• Impedance Converter



$$Z_{in} = \frac{V_i}{I_i} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$$

↙ Find out as exercize

Example

Design an active circuit inductor without using any inductance elements.

NOTE:

$$A_v = \frac{A_0}{1 + \beta A_0}$$

When dealing with op-amp we have always to cross check that two assumptions are true

$$\begin{cases} \beta A_0 >> 1 \\ V_0 < V_{SAT} \end{cases}$$

PRATICAL OP AMP

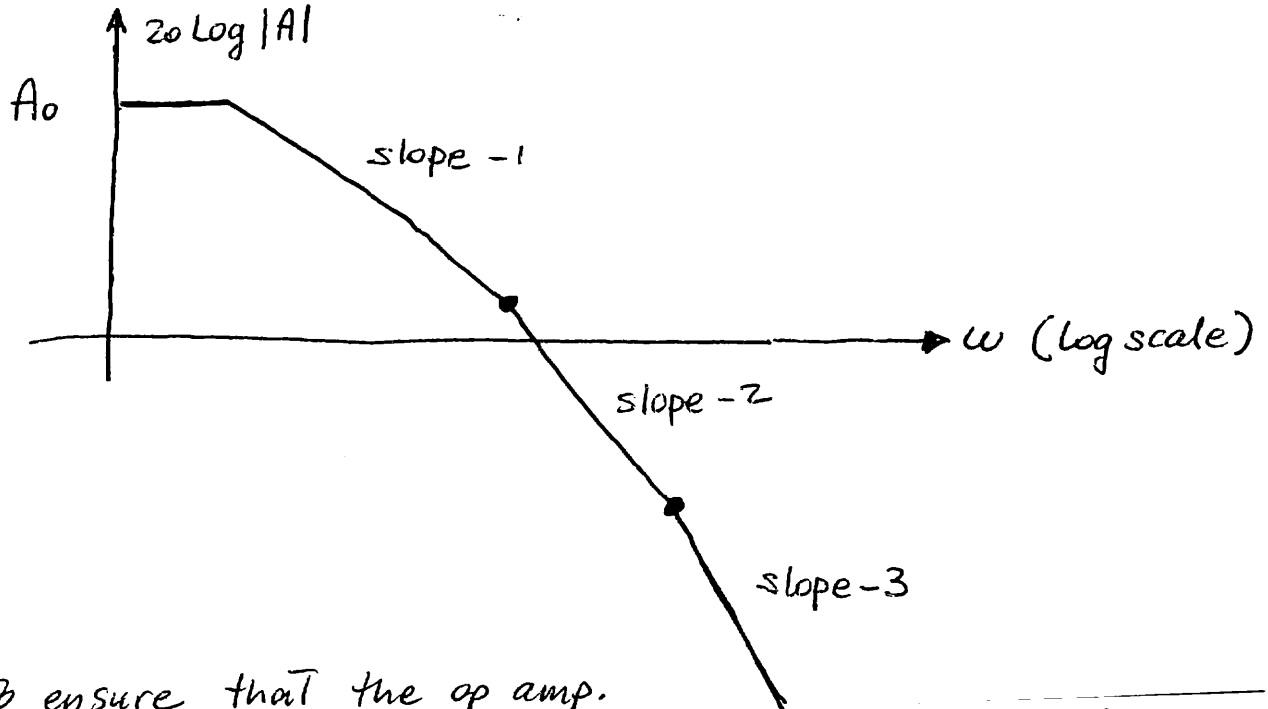
It's important to consider non ideal properties of op amp so that we can appreciate where are the limits of the assumptions we made so far (validity of the approximations done)

- Finite open loop gain
- Finite bandwidth
- output saturation
- slew rate
- DC Imperfections (offset voltage, current voltage)

OPEN LOOP GAIN AND BANDWIDTH

The open loop gain of an op amp is finite and decrease with frequency!

Although the gain is quite high at dc and low frequencies, it starts to fall off at a rather low frequency (due to the capacitances of the transistors inside the op. amp.)



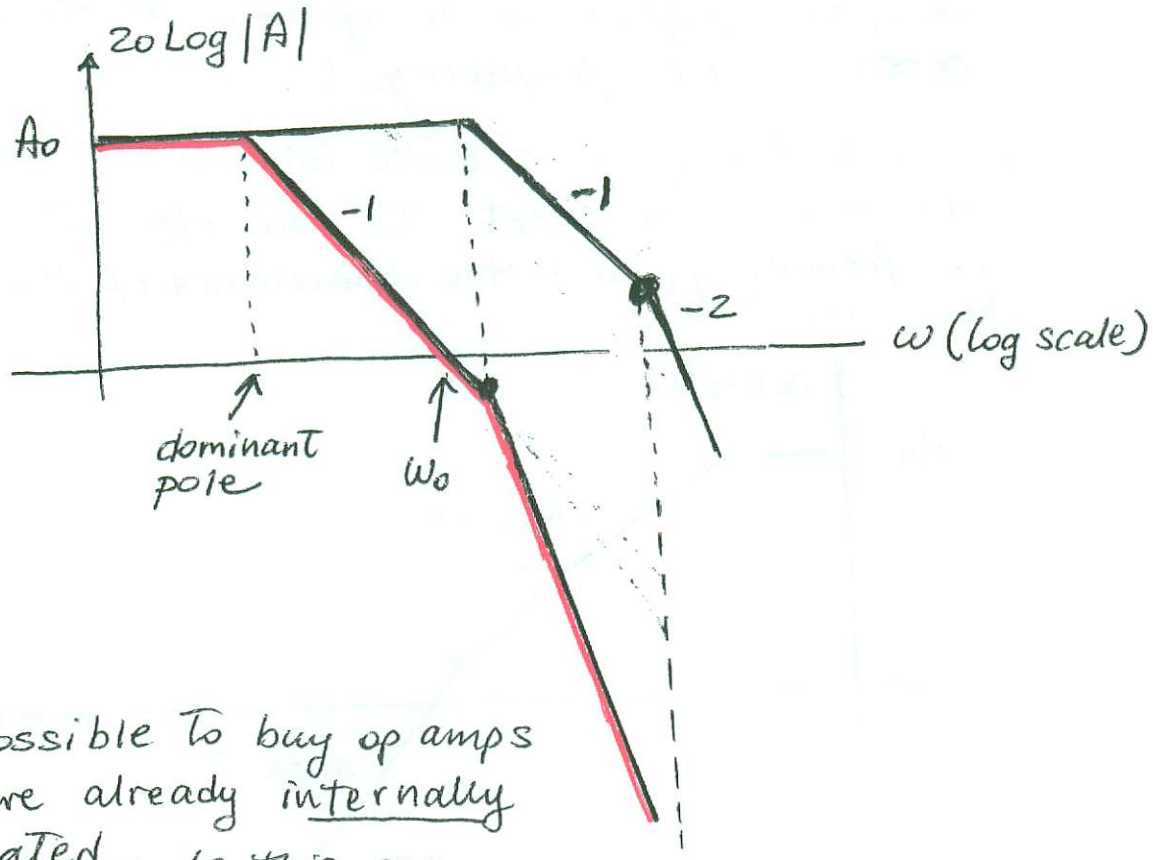
To ensure that the op amp. circuits will be <u>stable</u> (as opposed to oscillatory) we know from feedback theory that we to cut the unity gain axisis (0dB) with slope -1

In order to satisfy this "stability" requirement we need to modify the open-loop gain frequency response ⟹ frequency compensation

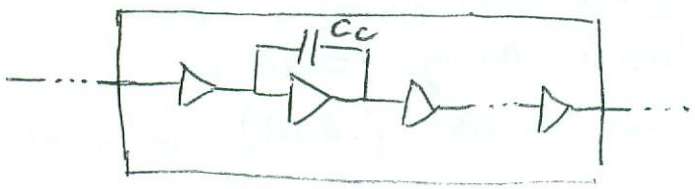
The frequency compensation process consists in introducing a pole (at a quite small frequency) so that it will "dominates" the amplifier frequency response.

↓

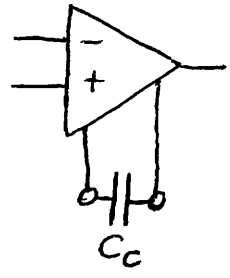
dominant pole



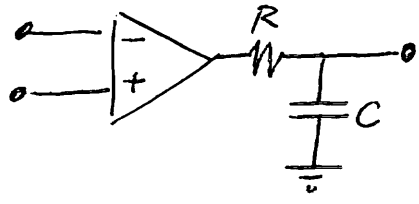
It's possible to buy op amps which are already internally compensated. In this case typically one of the high voltage gain stage has a feedback capacitance between input and output.



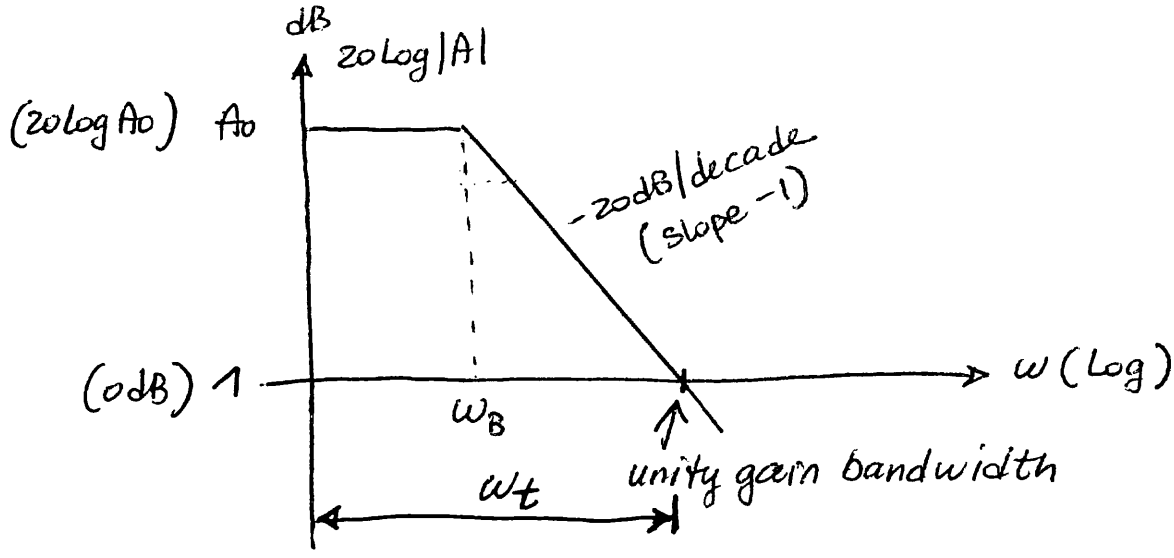
In other cases the manufacturer provides extra terminals where the compensation network can be inserted and shows as well how the open loop frequency response will be for different values of suggested compensation capacitance



If the manufacturer does not provide compensation it's up to the designer to implement compensation through its own external network.



It's important to look at the op-amp data sheet.



$$A(s) = \frac{A_o}{1 + s/\omega_B} \xrightarrow{s=j\omega} A(j\omega) = \frac{A_o}{1 + j\omega/\omega_B}$$

<u>at dc</u> : $\omega/\omega_B \ll 1 \rightarrow A(j\omega) \approx A_o$

<u>at high frequencies</u>: $\omega/\omega_B \gg 1 \rightarrow A(j\omega) \approx \frac{A_o}{j\omega/\omega_B}$

$$|A(j\omega)| = \frac{A_o \omega_B}{\omega}$$

$$20 \text{Log} \, |A(j\omega)| = 20 \text{Log} \, \frac{A_o \omega_B}{\omega} = 20 \text{Log} \, A_o \omega_B - 20 \text{Log} \, \omega =$$

$$= K - 20 \text{Log} \, \omega$$

↖ Line with negative slope of 20 dB per decade

At what frequency does the gain reach unity ?
(= when does the frequency response curve cut the 0 dB axis ?)

For $\omega \gg \omega_B \rightarrow 1 = \frac{A_o \omega_B}{\omega} \rightarrow \omega = A_o \omega_B \triangleq \omega_t$

↑ do not forget to check that !! (ω at least 10 times ω_B)

↑ unity gain bandwidth (Usually given on the data sheet !)

ω_B is called <u>break frequency</u> (or corner frequency) and it denotes the point of the frequency response where A rolled off 3dB from the dc gain A_0

$$A(j\omega) = \frac{A_0}{1 + \frac{j\omega}{\omega_B}} \underset{\omega=\omega_B}{=} \frac{A_0}{1+j}$$

$$|A(j\omega_B)| = \frac{A_0}{\sqrt{2}}$$

$$20\log\frac{1}{\sqrt{2}} = -20\log\sqrt{2} = -3dB$$

Effect of finite open loop gain and frequency response on the closed loop amplifiers

INVERTING AMPLIFIER

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1+\frac{(1+R_2/R_1)}{A}} = \frac{-R_2/R_1}{1+\frac{(1+R_2/R_1)}{\frac{A_o}{1+s/\omega_B}}} =$$

$$= \frac{-R_2/R_1}{1+\frac{(1+R_2/R_1)(1+s/\omega_B)}{A_o}} =$$

$$= \frac{-R_2/R_1}{1+\frac{1+R_2/R_1}{A_o}+\frac{(s/\omega_B)(1+R_2/R_1)}{A_o}} =$$

$$= \frac{-R_2/R_1}{1+\frac{1+R_2/R_1}{A_o}+\frac{(1+R_2/R_1)\,s}{A_o\omega_B}} = \qquad \text{(circled } A_o\omega_B = \omega_t\text{)}$$

$A_o \gg 1+\frac{R_2}{R_1}$

$$\simeq \frac{-R_2/R_1}{1+(1+R_2/R_1)\frac{s}{\omega_t}}$$

$$\downarrow$$

$$G_{dc} = -R_2/R_1$$

$$\omega_{3dB} = \frac{\omega_t}{1+R_2/R_1}$$

← it means that we want the denominator to become $1+j$

NON INVERTING AMPLIFIER

$$\frac{V_o}{V_i} = \frac{1+R_2/R_1}{1+\frac{(1+R_2/R_1)}{A}} = \frac{1+R_2/R_1}{1+\frac{1+R_2/R_1}{A_o}+\frac{(1+R_2/R_1)s}{\omega_B A_o}} =$$

$$= \frac{1+R_2/R_1}{1+\frac{1+R_2/R_1}{A_o}+\frac{s}{\omega_t}(1+R_2/R_1)} \overset{\uparrow}{=}$$

$1+R_2/R_1 \ll A_o$

$$\simeq \frac{1+R_2/R_1}{1+(1+R_2/R_1)\frac{s}{\omega_t}}$$

$\downarrow$

$$G_{dc} = 1+\frac{R_2}{R_1}$$

$$\omega_{3dB} = \frac{\omega_t}{1+\frac{R_2}{R_1}}$$

Example

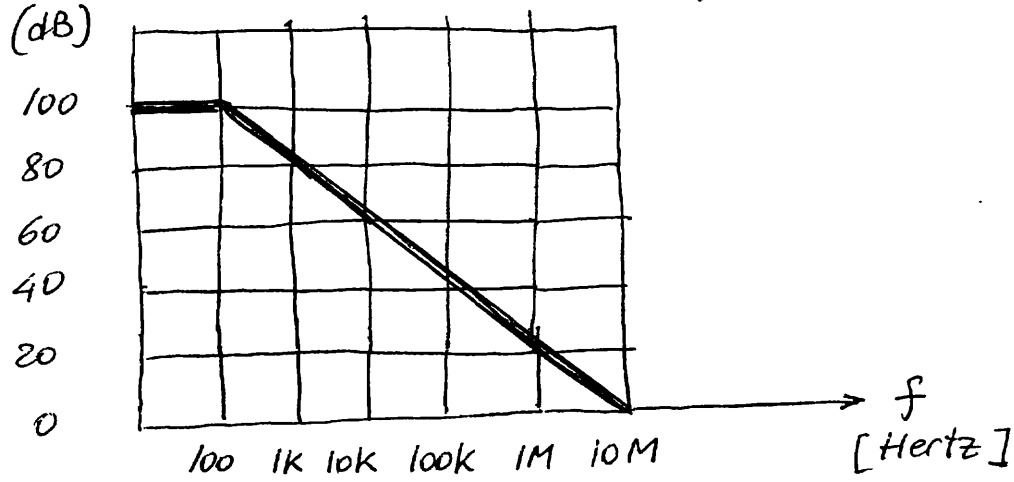
Design an amplifier with:

$A_v = 1000$ (60 dB)

$BW = 100$ KHz

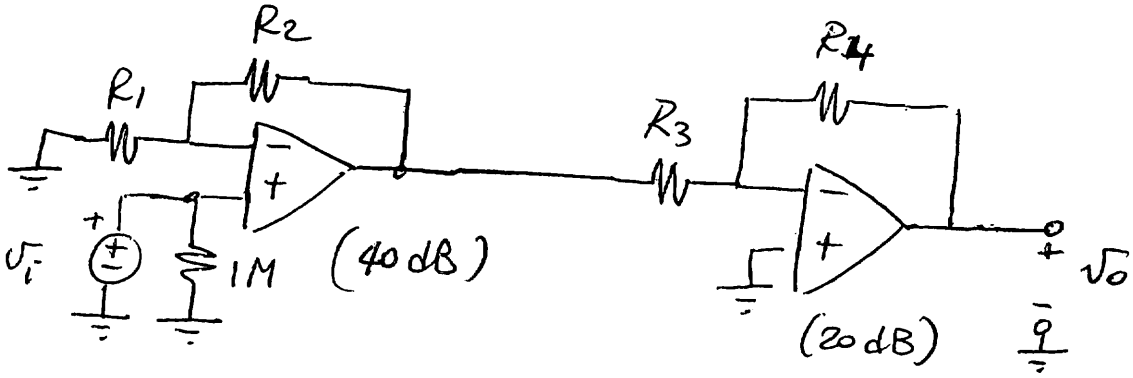
$R_{in} = 1\ M\Omega$

I have available this op amps



It's impossible to put together 60 dB of gain and a BW = 100 KHz using only a single op-amp.

We have to partition the gain over more op amps.



LARGE SIGNAL OPERATION OF OP AMPS

- SATURATION
- SLEW RATE (FULL POWER BANDWIDTH)

Saturation

op amps operate linearly only over a limited range of output voltage.
op amp output saturates within 1 to 3 volts of the positive and negative power supply

$$-V_{SAT} \leq v_o \leq +V_{SAT}$$

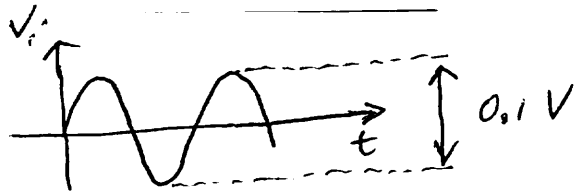
$\mp V_{SAT}$ is called rated output voltage or output voltage swing

In order to avoid clipping off the peaks of the output waveform (and the resulting waveform distorsion) the input signal must be kept correspondingly small.

Example

rated output voltage = $\pm 10V$
gain = 200
what is the largest sine wave input that can be handled ?

$$V_{i\,max} = \frac{20}{200} = 0.1\,V \quad \text{peak-to-peak}$$



SLEW RATE

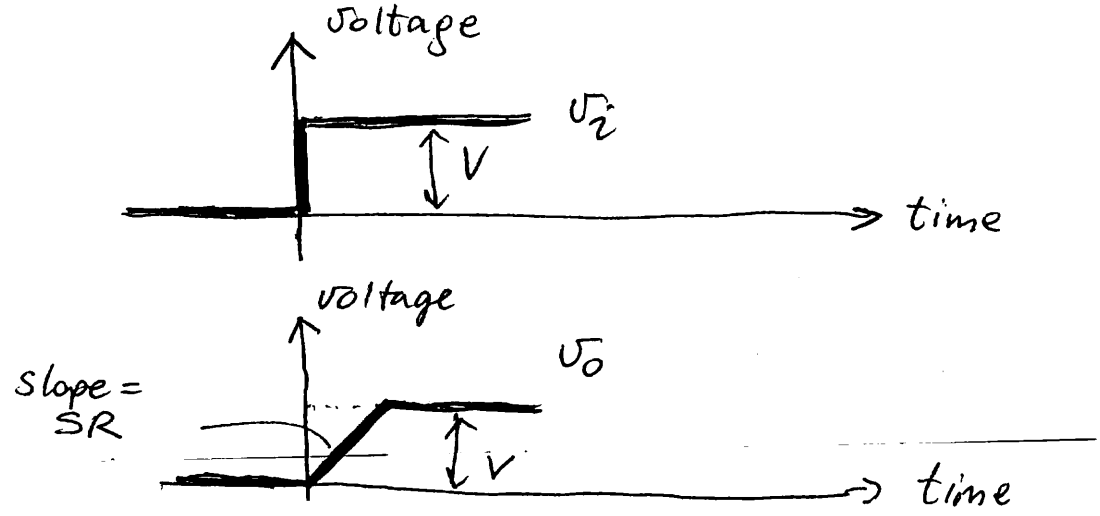
The slew rate describes another large-signal limitation phenomenon (that can cause non-linear distortion when large output signals are present) of op-amps.

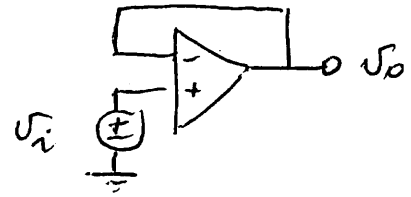
Slew rate is a measure of the speed at which the output signal can change.
It is defined as the maximum time rate of change possible at the output voltage of the op amp.

$$SR = \left.\frac{dV_o}{dt}\right|_{max}$$

→ It's usually specified on the op-amp data sheet in units of V/μs

If the input signal applied is such that demands an output response that is faster than the specified value of SR the op amp will not comply.





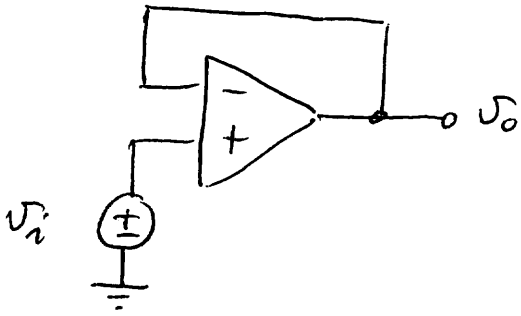
phenomenon

Slew rate limiting occurs because of the capacitive elements inside the op amp (specially the compensation capacitance).
It takes time to charge and discharge capacitances, so the op amp is not able to respond instantaneously to changes in the input signal !!

Effect of slew rate (POWER BANDWIDTH)

Let's consider a unity gain voltage follower with a sine wave input:

$$v_i = V_i \sin \omega t$$

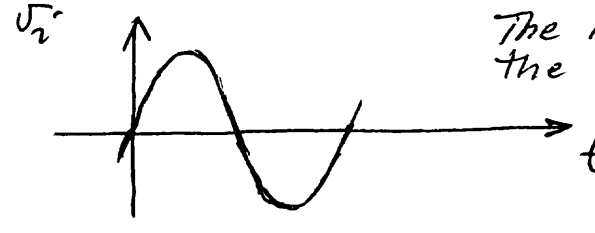


The rate of change of this waveform is:

$$\frac{dv_i}{dt} = \omega V_i \cos \omega t$$

↓ max rate of change

$$\left.\frac{dv_i}{dt}\right|_{max} = \omega V_i \underbrace{\cos \omega t}_{1} = \omega V_i$$



The maximum occurs at the zero crossings of the input sinusoid.

If ωV_i exceeds the slew rate of the op amp the output waveform will be distorted → the output cannot keep up with the large rate of change of sinusoid at its zero crossings and the op-amp slews.

The op-amp data sheets usually specify a frequency called <u>Full power bandwidth</u> f_p that is defined as the frequency at which a sine wave output, at rated output voltage starts to experience distorsion

$$SR = 2\pi f_p V_{o_{max}}$$

$$\downarrow$$

$$f_p = \frac{SR}{2\pi V_{omax}} \leftarrow \text{POWER BANDWIDTH}$$

The goal is satisfy:

$$SR \geq \omega_p V_{omax}$$

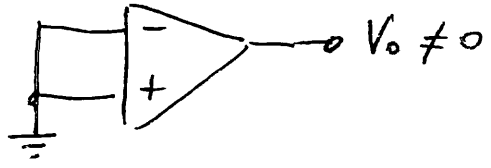
It's clear that if the output sinusoids are of amplitude smaller than V_{omax} we have slew rate distorsion only at frequency higher than ω_p

DC IMPERFECTIONS (OFFSET VOLTAGES and CURRENTS)

- input offset voltage
- input bias current (→ input offset current)

An ideal op amp is perfectly balanced that is $V_o = 0$ when $V_1 = V_2 = 0$.

Unfortunately a real op amp exhibits an imbalance caused by the fact that there is always a sligth mismatch in the input transistors of the op-amp. (differential stage)



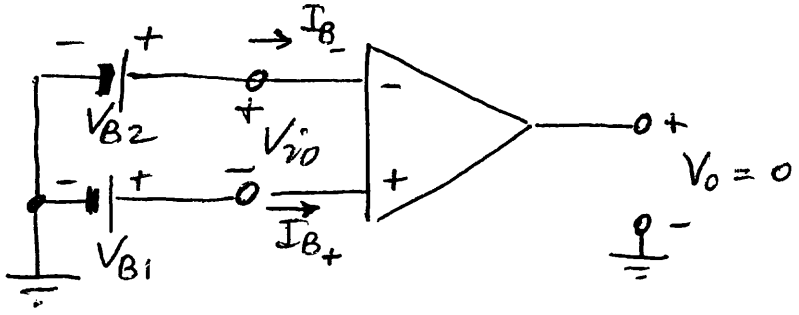
This mismatch results in unequal bias currents in the input terminals and unequal Base-emitter voltages.

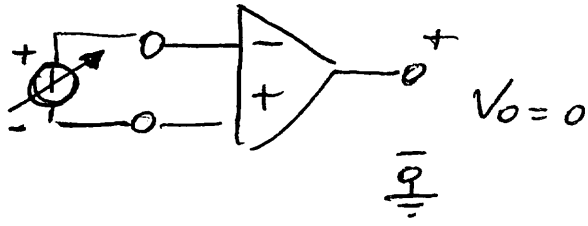
- OFFSET VOLTAGE

As consequence if the two input terminals of the op amp are tied together and connected together to ground it will be found that a finite (quite small) dc voltage exists at the output.

Pratically this means that whenever I apply an input signal v_i then at the output I will have the desired output signal v_o plus a small dc residual V_o.

The op amp can be brought back to its ideal value of 0V by connecting a dc voltage source of appropriate polarity and magnitude between the two input terminals of the op amp. !!
For the external source to balance out "the input offset voltage" of the op. amp. (V_{io})
it must be of equal magnitude and opposite polarity of the input voltage offset V_{io})





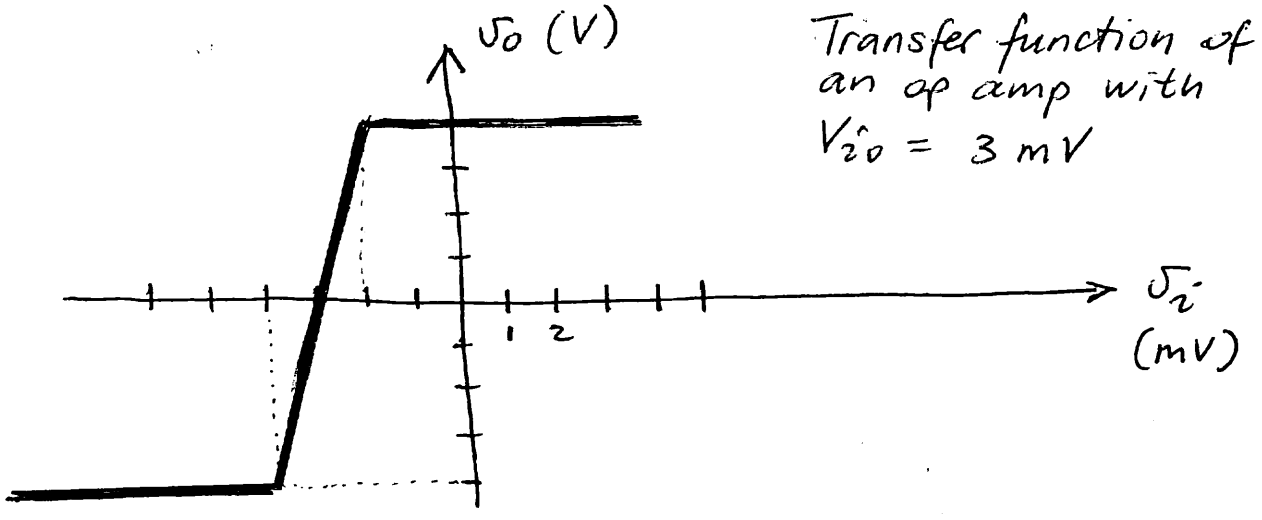
Op-amps exhibit a V_{io} in the range of $1 \div 5$ mV.
Also the value of V_{io} depends on temperature
Usually data sheets specify typical and max values of V_{io} at room temperature
as well as how the V_{io} drift with the temperature
($\frac{\Delta V_{io}}{\Delta T}$ → order of $\mu V/^{\circ}C$)

The data sheet specify the V_{io} value, however they do not specify the polarity ($\rightarrow$ we cannot know "a priori" the "direction" of the transistors mismatch)

$\downarrow$

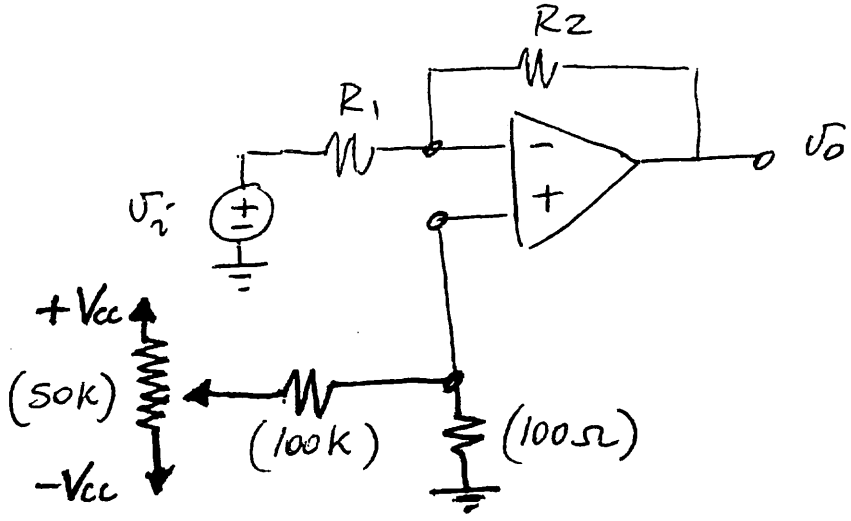
to balance the offset we need to proceed experimentally !!

Since it is a problem to find small dc voltage sources (mV magnitude) usually the offset calibration is done through "ad hoc" circuits

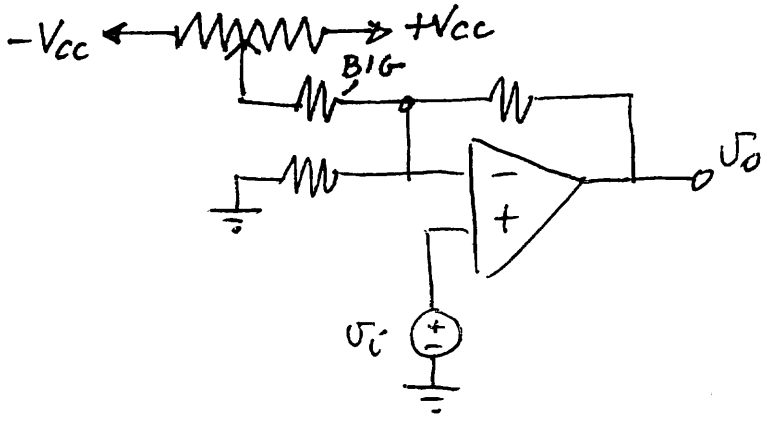


Transfer function of an op amp with $V_{io} = 3$ mV

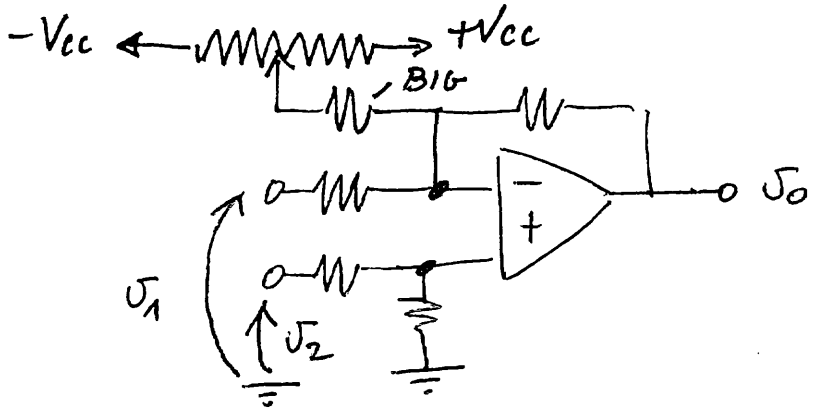
Universal output offset-voltage balancing circuits:



INVERTING CONFIGURATION



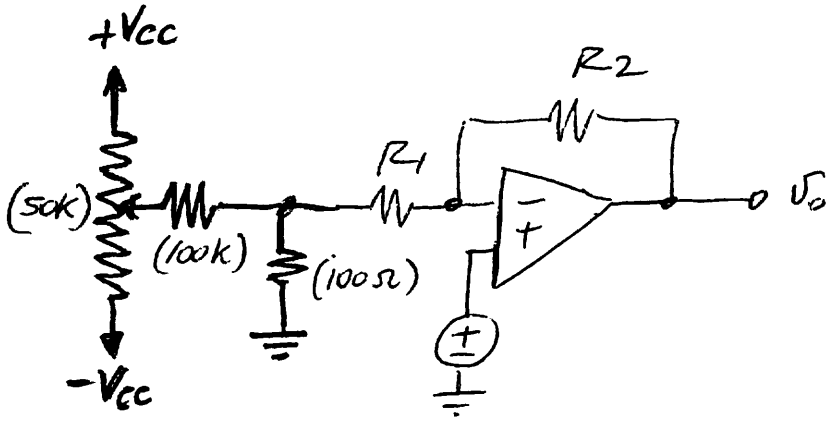
NON INVERTING CONFIGURATION



MIXED CONFIGURATION

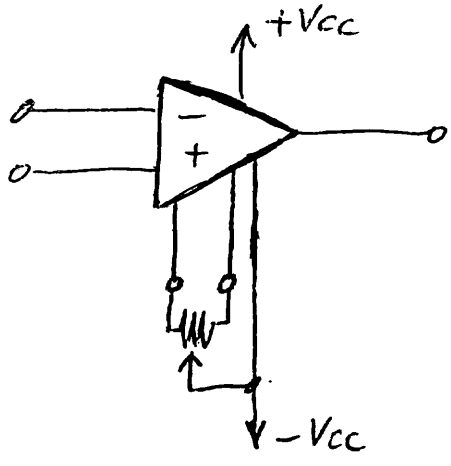
There many other reasonable balancing circuits that can be built !!

You can make up your own or follow the advices on the data sheets (→ which is probably the wiser way to go !!)



ANOTHER NON INVERTING CONFIGURATION

There are op-amp manufacturers provide two extra terminals for offset nulling



The way to proceed to trim the offset voltage to zero is as follow:

1. we build the circuit we want to implement
2. we put the input terminals to ground
3. we move the potentiometer wiper until v_o is zero

INPUT BIAS CURRENTS

In order for the op amp to operate its two input transistors have to be biased (the differential amplifier transistors). There may be dc currents flowing at the inputs of the op-amp.

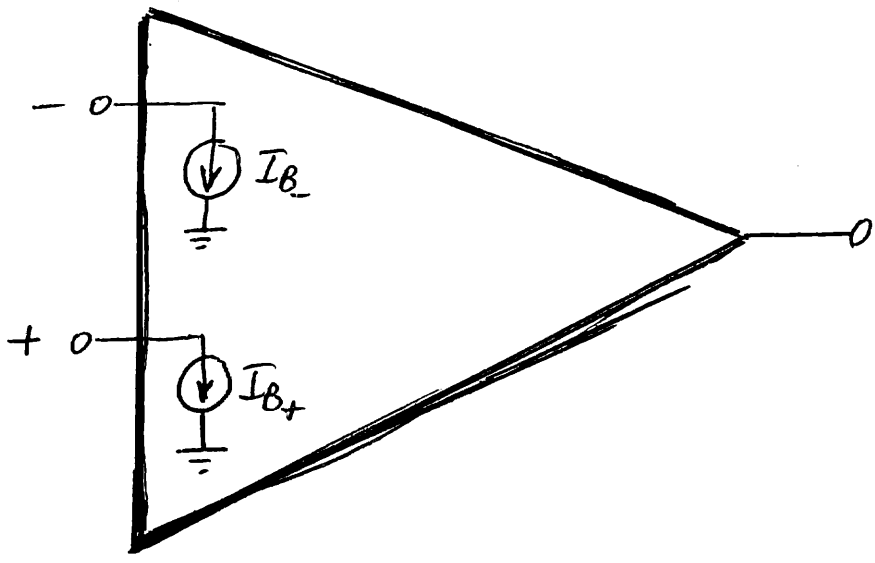
- there are always dc currents if the differential stage is done with BJT
- there are almost no dc currents if the differential stage is done with ~~FET~~ → unless I deal with a single power supply op-amp that has an internal biasing network to move the operating point at Vcc/2 (→ not very common)

Those possible dc currents are termed the INPUT BIAS CURRENTS.

The op-amps manufacturer usually specify the average value of I_{B+} and I_{B-} as well as their expected difference:

$$I_{BIAS} = \frac{I_{B+} + I_{B-}}{2}$$ ← INPUT BIAS CURRENT

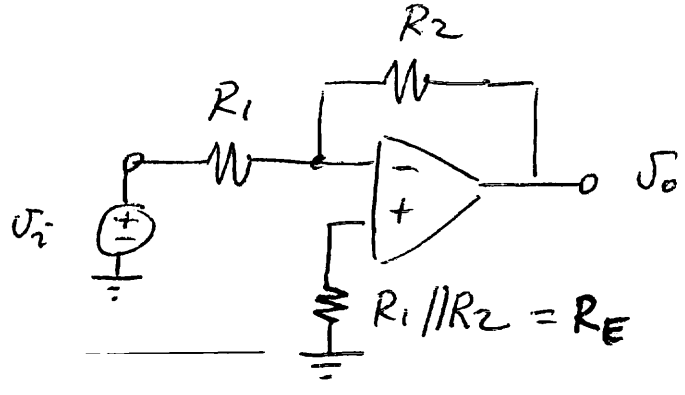
$$I_{io} = \left| I_{B+} - I_{B-} \right|$$ ← INPUT OFFSET CURRENT



Typical values of offset current are of the order of 10 nA for op-amps that use BJT and of the order of pA for op-amps that use FET.

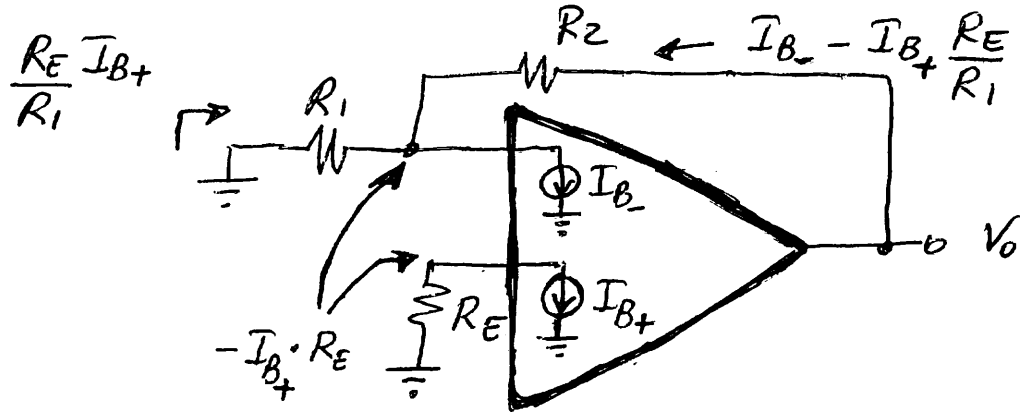
The input offset current I_{io} depends on temperature so usually the manufacturers specify as well the input offset current drift ($\frac{\Delta I_{io}}{\Delta T}$ → order of nA/°C)

Let's see how we can get rid of the current offset !!

① 

INVERTING-CONFIGURATION

if we ground the signal source we obtain the following :



$$V_o = R_2 \cdot \left(I_{B-} - I_{B+} \frac{R_E}{R_1} \right) - I_{B+} \cdot R_E =$$

$$= R_2 I_B - I_B \frac{R_E}{R_1} \cdot R_2 - I_B R_E =$$

$$= I_B \left(R_2 - \frac{R_E}{R_1} \cdot R_2 - R_E \right) =$$

$$= I_B \left(R_2 - R_E \left(1 + \frac{R_2}{R_1} \right) \right)$$

$I_{B+} \approx I_{B-} \approx I_B$

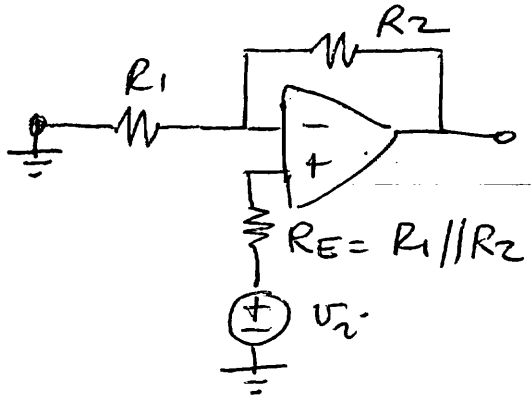
$$\begin{cases} I_{B+} = I_B + \frac{I_{io}}{2} \\ I_{B-} = I_B - \frac{I_{io}}{2} \end{cases}$$

To reduce $V_o = 0$ we select:

$$R_2 - R_E \left(1 + \frac{R_2}{R_1} \right) = 0$$

$$R_E = \frac{R_2}{1 + \frac{R_2}{R_1}} = \frac{R_1 R_2}{R_1 + R_2}$$

(2)



NON INVERTING CONFIGURATION

Summary of op-amps parameters

- Input offset voltage: V_{io}
  is that voltage which must be applied between the input terminals to balance the amplifier
- Input offset voltage drift: $\Delta V_{io}/\Delta T$
  is the ratio of the change of input offset voltage to the change in temperature
- output offset voltage
  is the dc voltage at the output terminal when the two input terminals are grounded
- Input bias current: I_B
  is $\frac{1}{2}$ of the sum of the separate currents entering the input terminals of a balanced amplifier: $I_B = \frac{I_{B+} + I_{B-}}{2}$ when $V_o = 0$
- Input offset current: I_{io}
  is the difference between the separate currents entering the input terminals of a balanced amplifier:

$$I_{io} = I_{B-} - I_{B+} \quad \text{when } V_o = 0$$

- input offset current drift: $\Delta I_{io}/\Delta T$
  is the ratio of the change of input current current to the change of temperature

- **Input differential range**
  The maximum difference signal that can be applied safely to the op-amp terminals

- **Output voltage range**
  The maximum output swing that can be obtained without significant distorsion

- **Full power bandwidth**
  The matimum frequency at which a sinusoids whose size is the output voltage range is obtained

- **Slew rate**
  is the time rate change of the output voltage under large signal conditions

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NOTE:
The offset balancing is usually done after the circuit has been working for a couple of hours !!!